

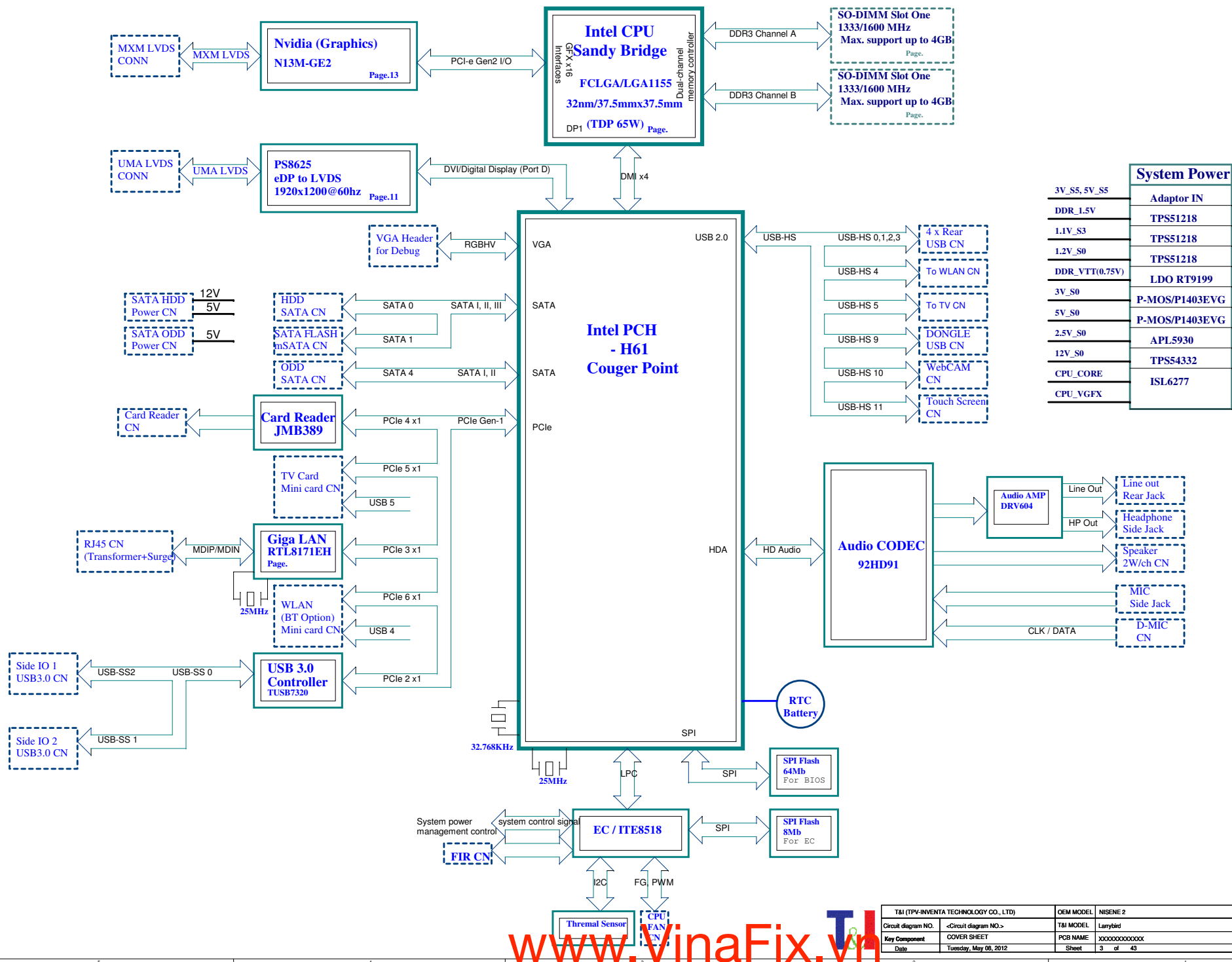
# TPV-INVENTA TECHNOLOGY CO., LTD. (TNI)

RDC2. EE Div. HW Department II

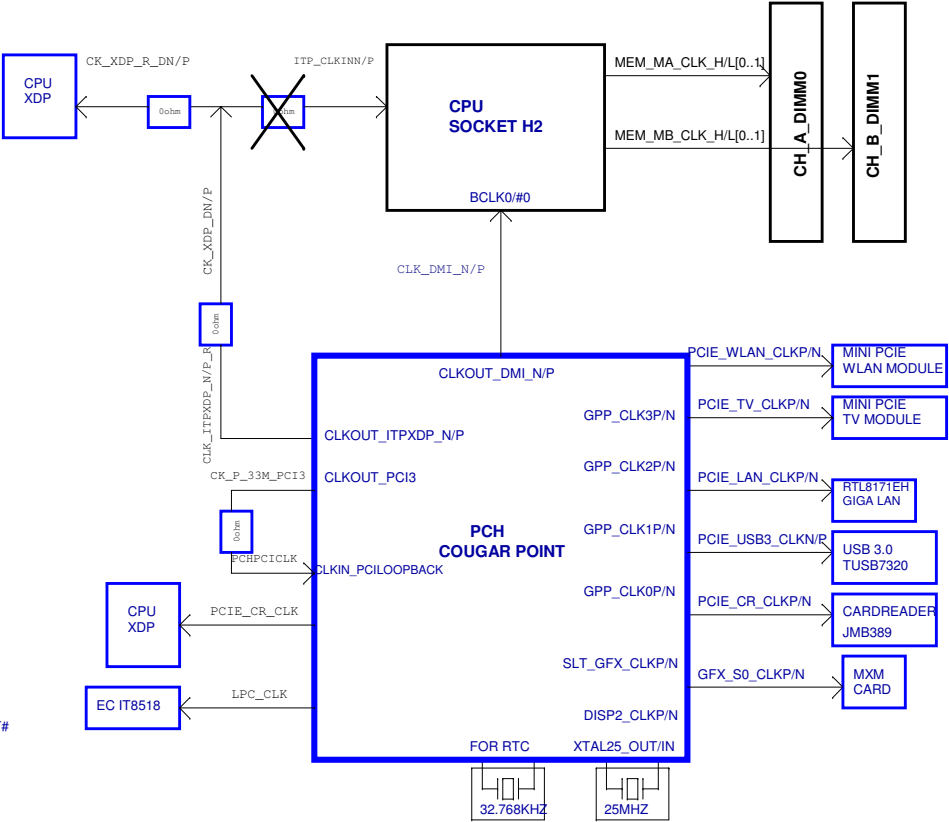
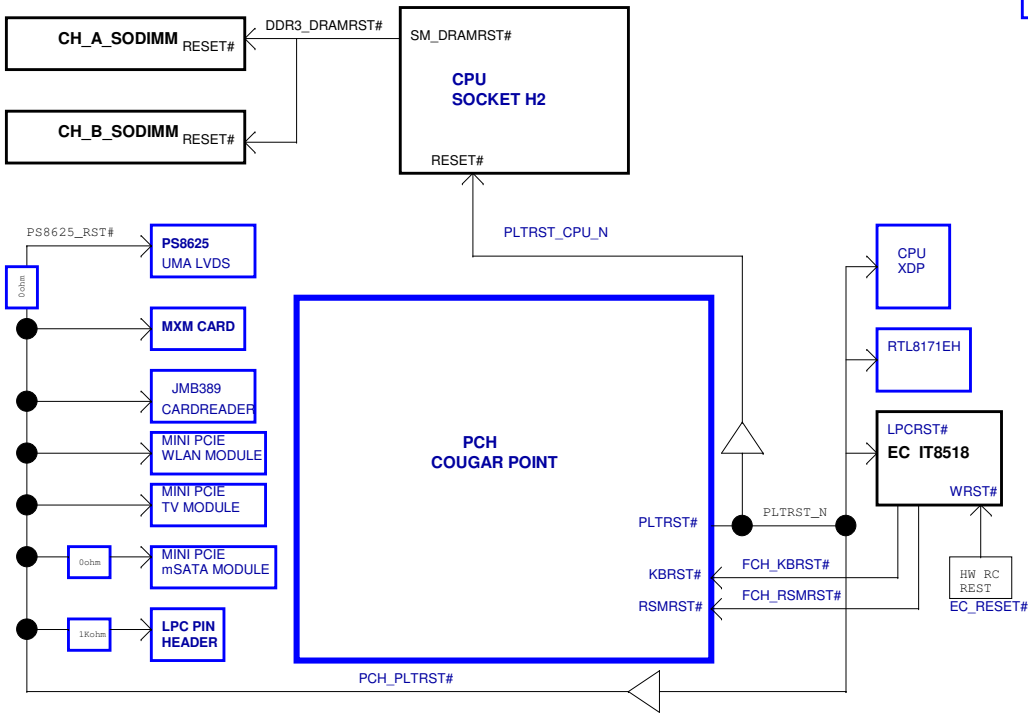
Board name : MotherBoard Schematic  
Project : Nell (Nisene2 LarryBird)  
Version : M0C  
Initial Date : 2012/02/10  
PCB P/N. : 6050A2516301  
PCBA P/N. : 1310A2516301



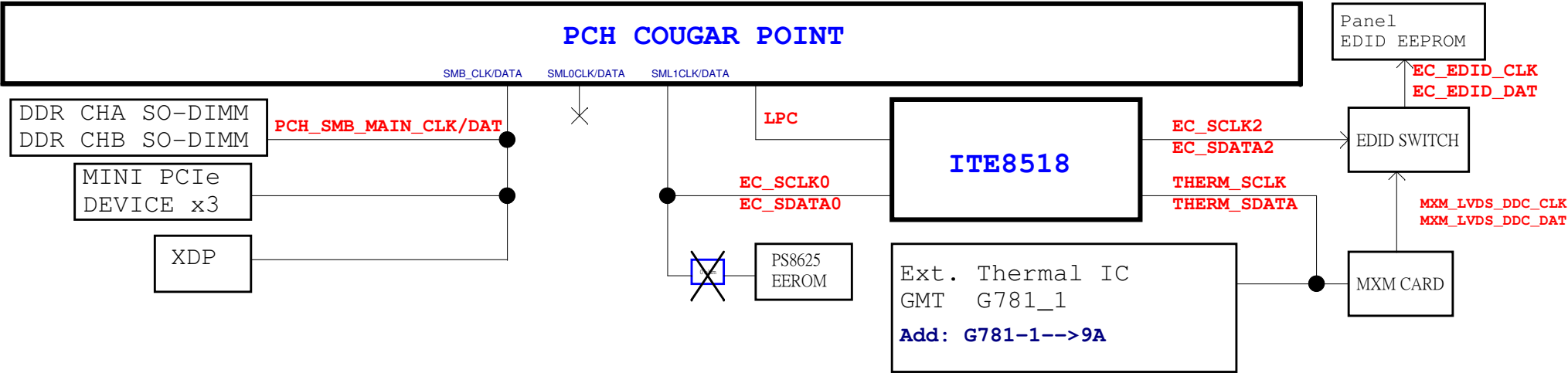
### 03 SYSTEM BLOCK DIAGRAM



RESET Block Diagram



SM Bus MAP

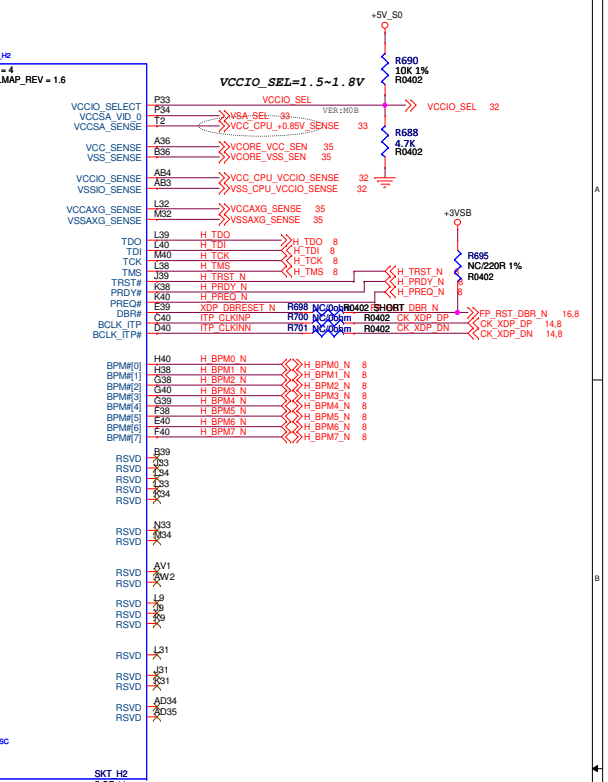
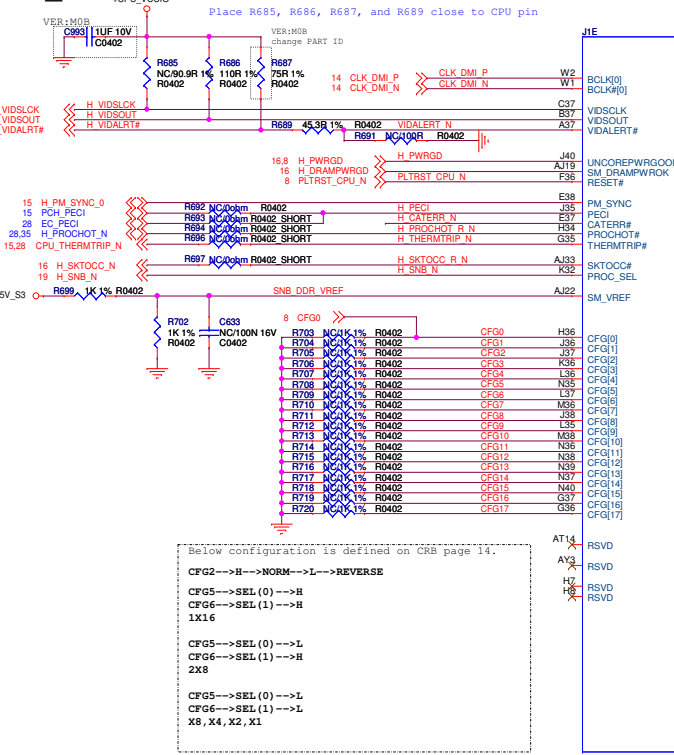


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	4 of 43	<remark>

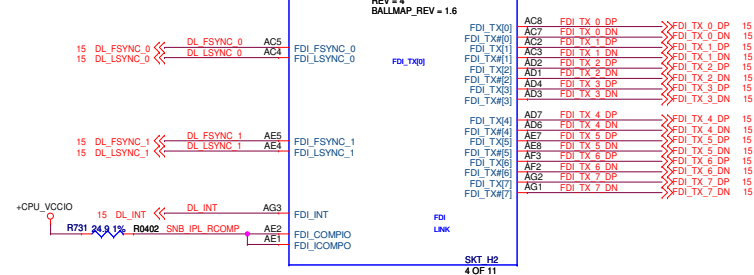
## PCIEX16 & DMI



## H2\_E

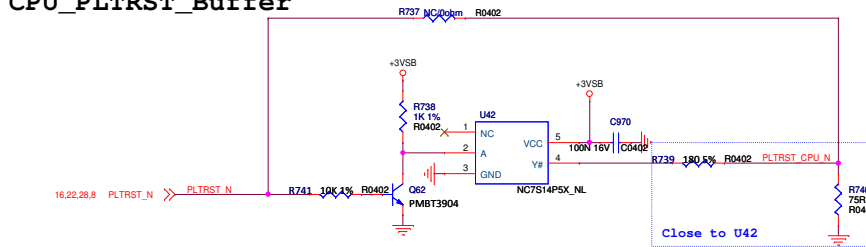


## FDI

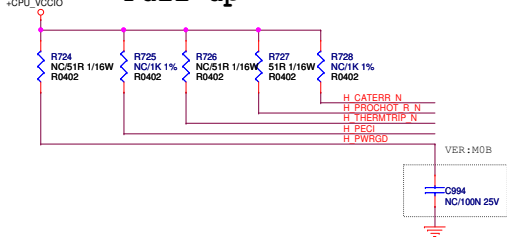


## CPU\_PLTRST Buffer

If PLTRST driver current enough, need to use buffer

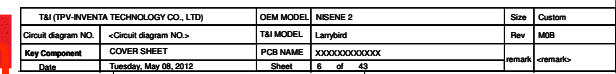


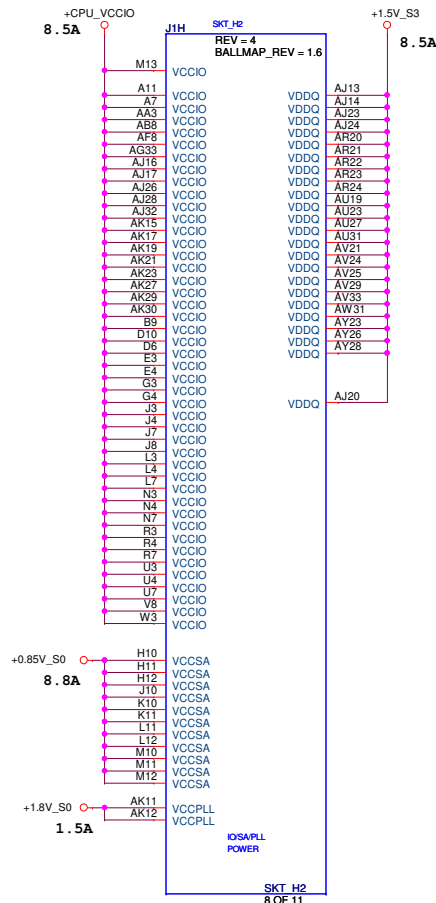
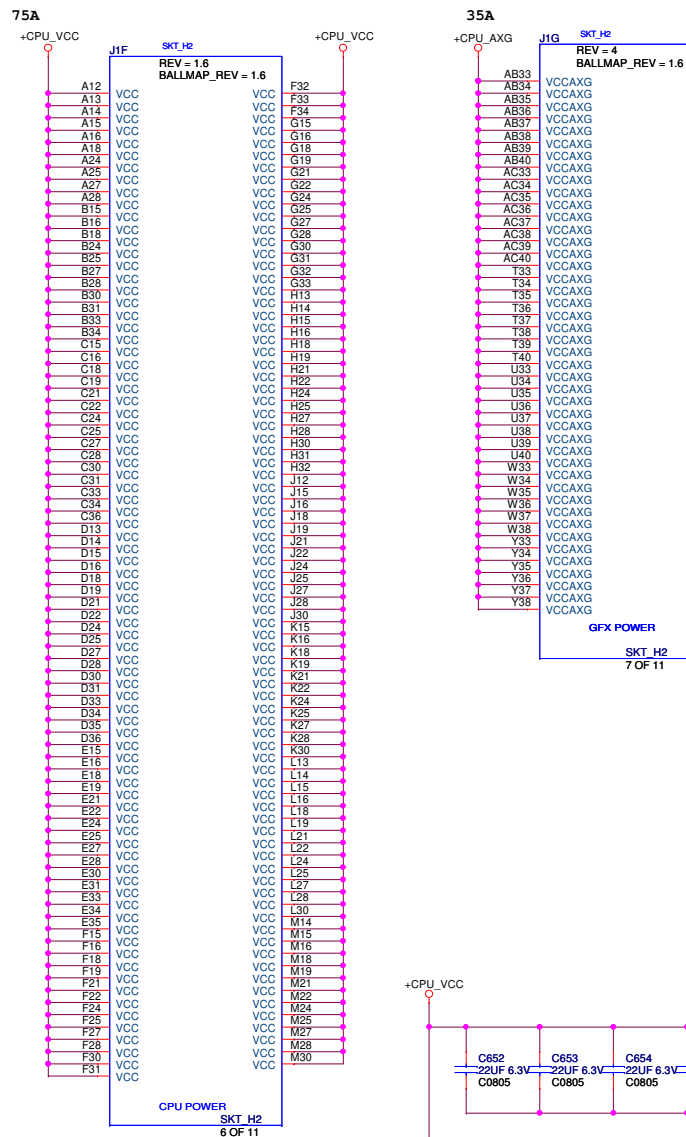
## Pull up



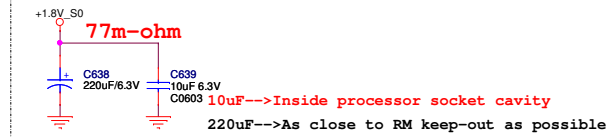
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	X00000000000	remark
Date	Tuesday, May 06, 2012	Sheet	5 of 43	<remark>

Channel\_B

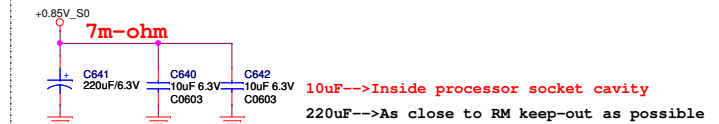




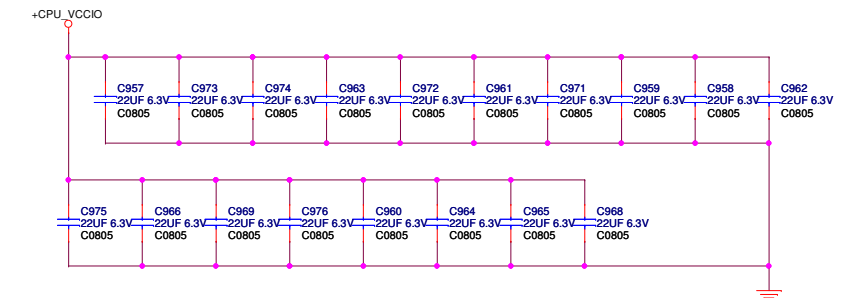
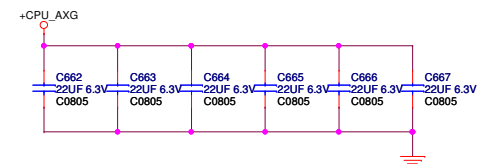
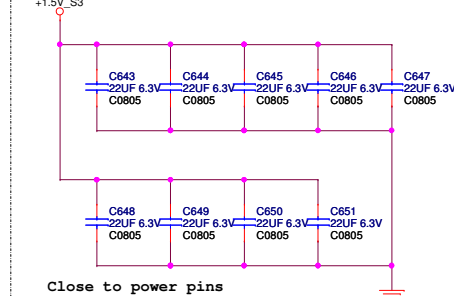
### +1.8V\_S0-->Decoupling



### +0.85V\_S0-->Decoupling



### +1.5V\_S0-->Decoupling



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	7 of 43	<remark>

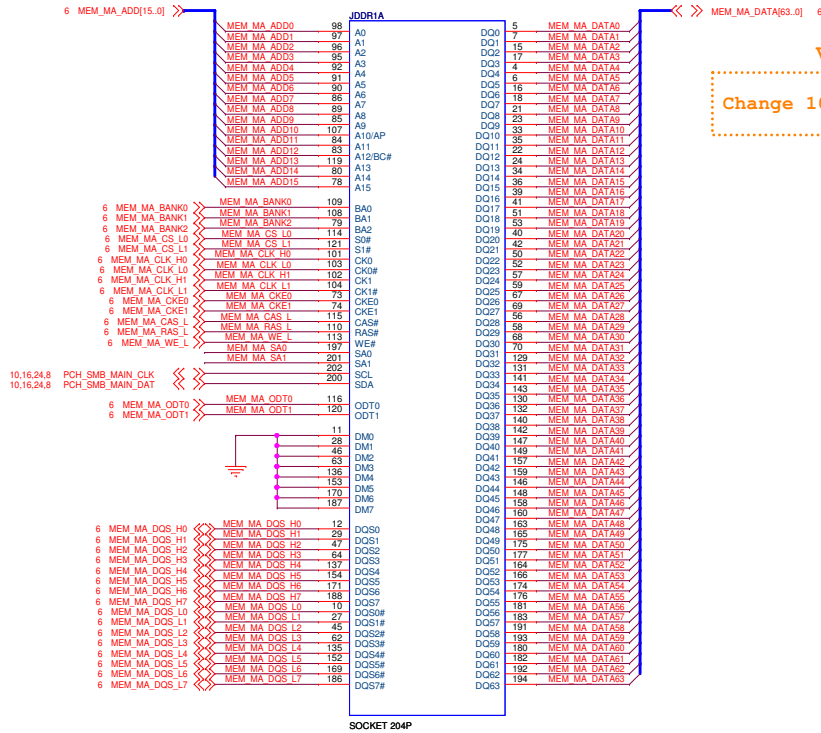




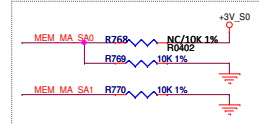


VER:MOB  
JDDR1 is change to 10.1mm height

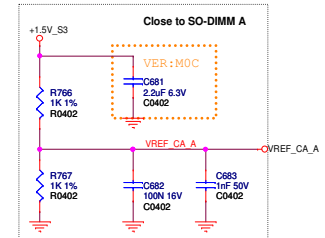
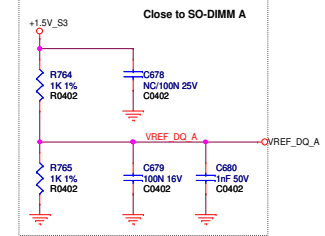
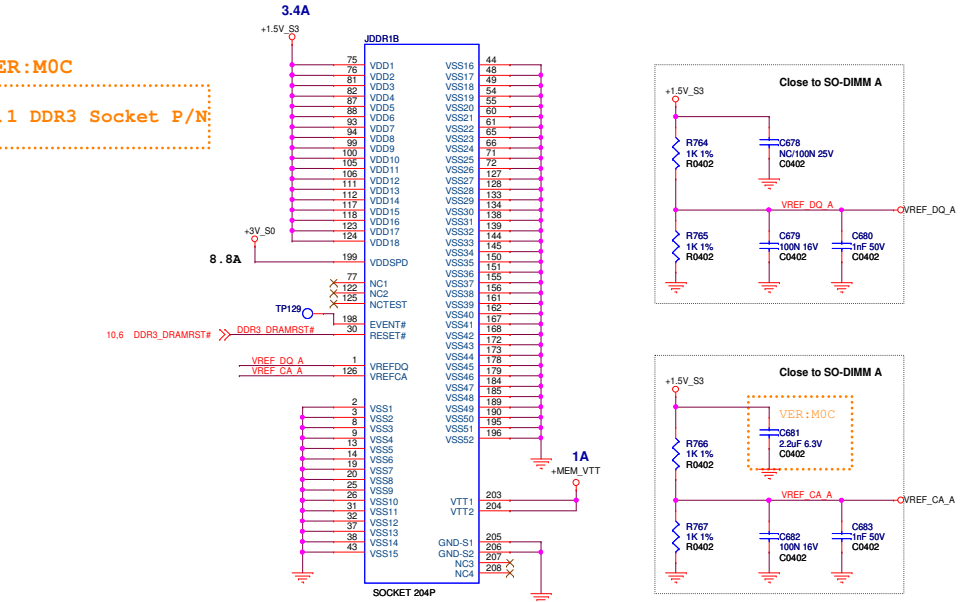
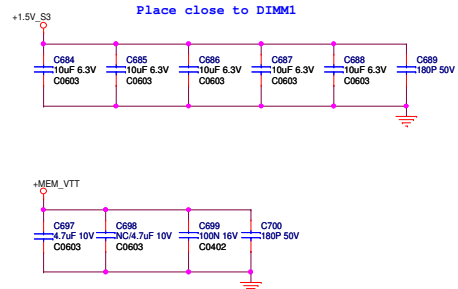
# CHA DDR 10.1H(DIMM-1)



DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

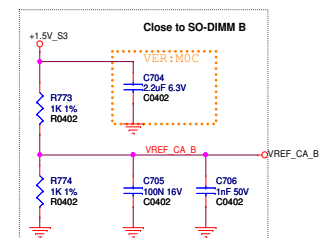
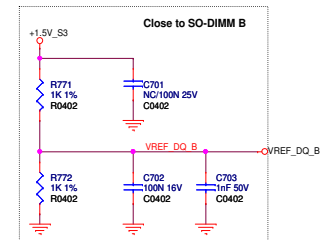
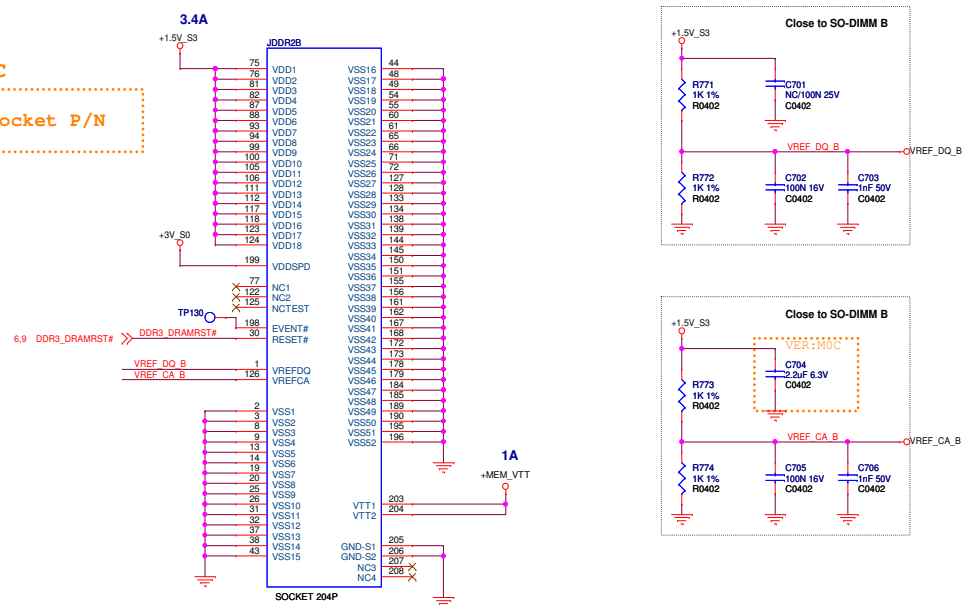
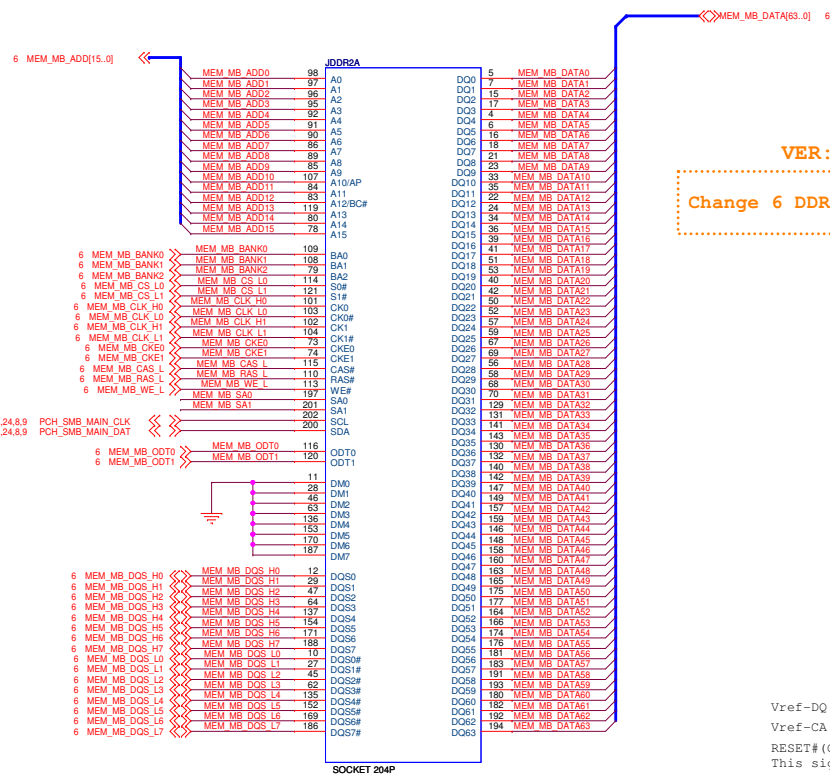


Note:  
If SA0 = 0, SA1 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
If SA0 = 1, SA1 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

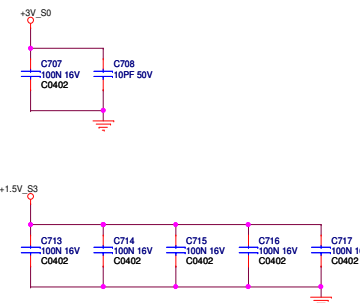
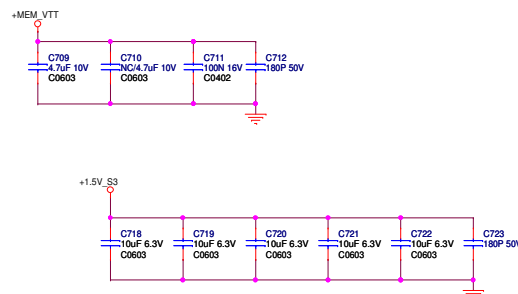
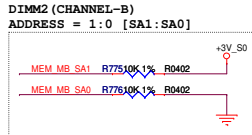


VER:M0B  
JDDR1 is change to 6.0mm height

# CHB DDR 6.0H(DIMM-2)



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR\_IN. When in single ended mode used for DQS0-DQS7.  
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.  
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW.  
This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

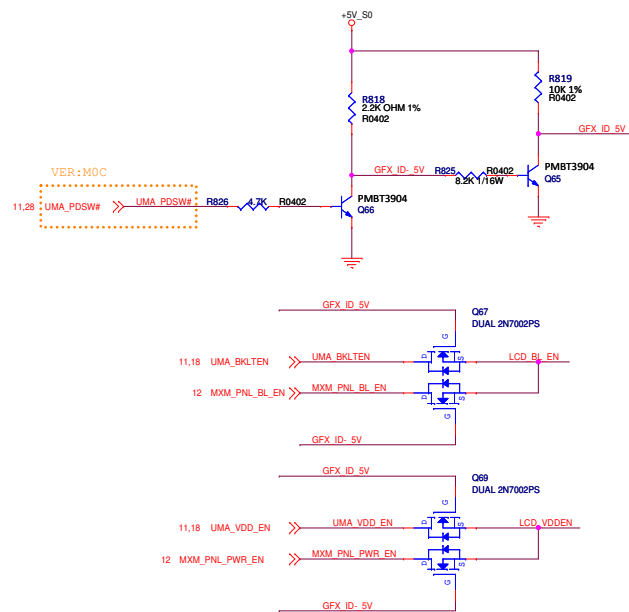


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	10 of 43	<remark>

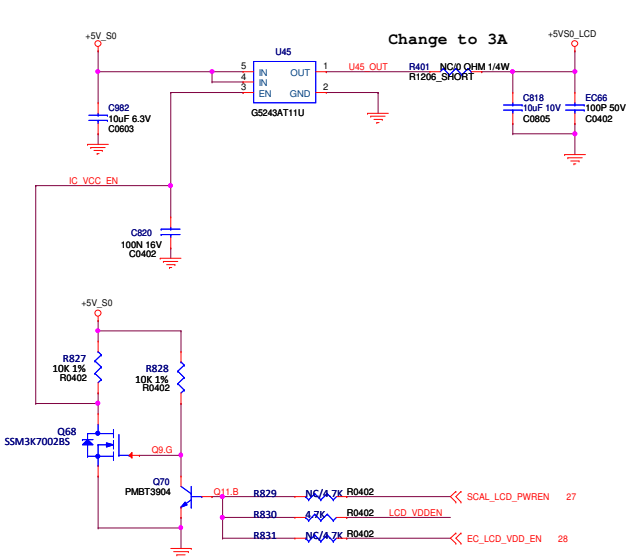




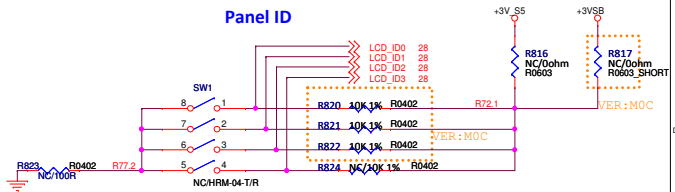
MXM & UMA BACKLIGHT ENABLE AUTO SELECT



LCD POWER ENABLE

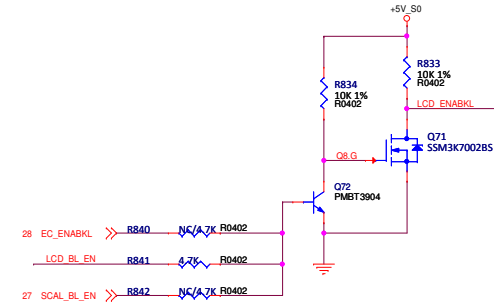


Panel ID

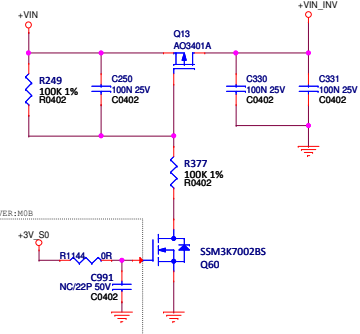
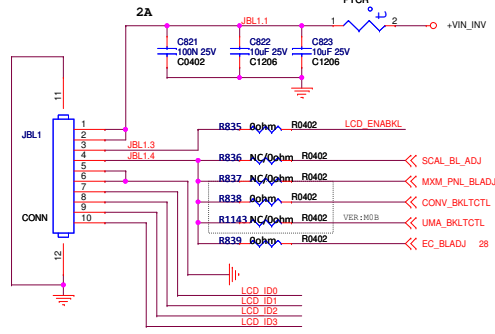


ID3	ID2	ID1	ID0	Panel
0	0	0	0	Samsung
0	0	0	1	LG
0	0	1	0	CMI
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	

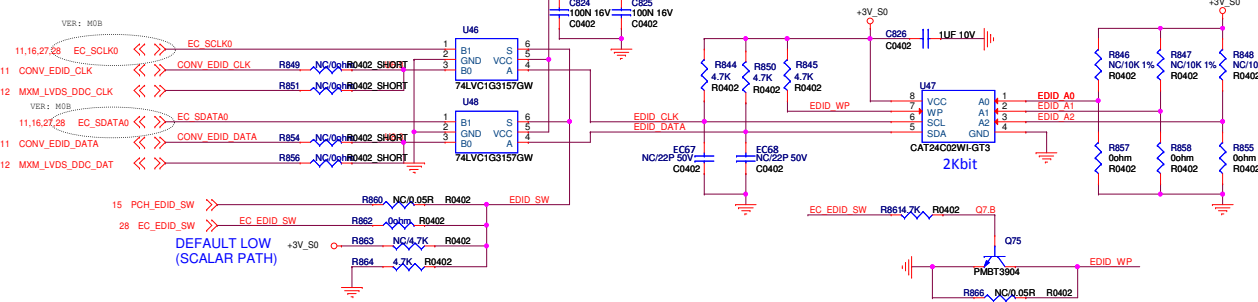
BACKLIGHT ENABLE



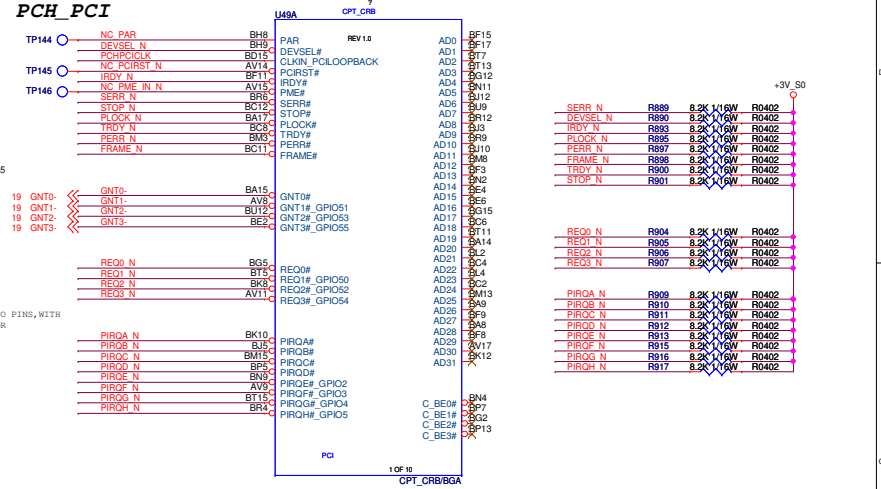
CONVERTER CONNECTOR



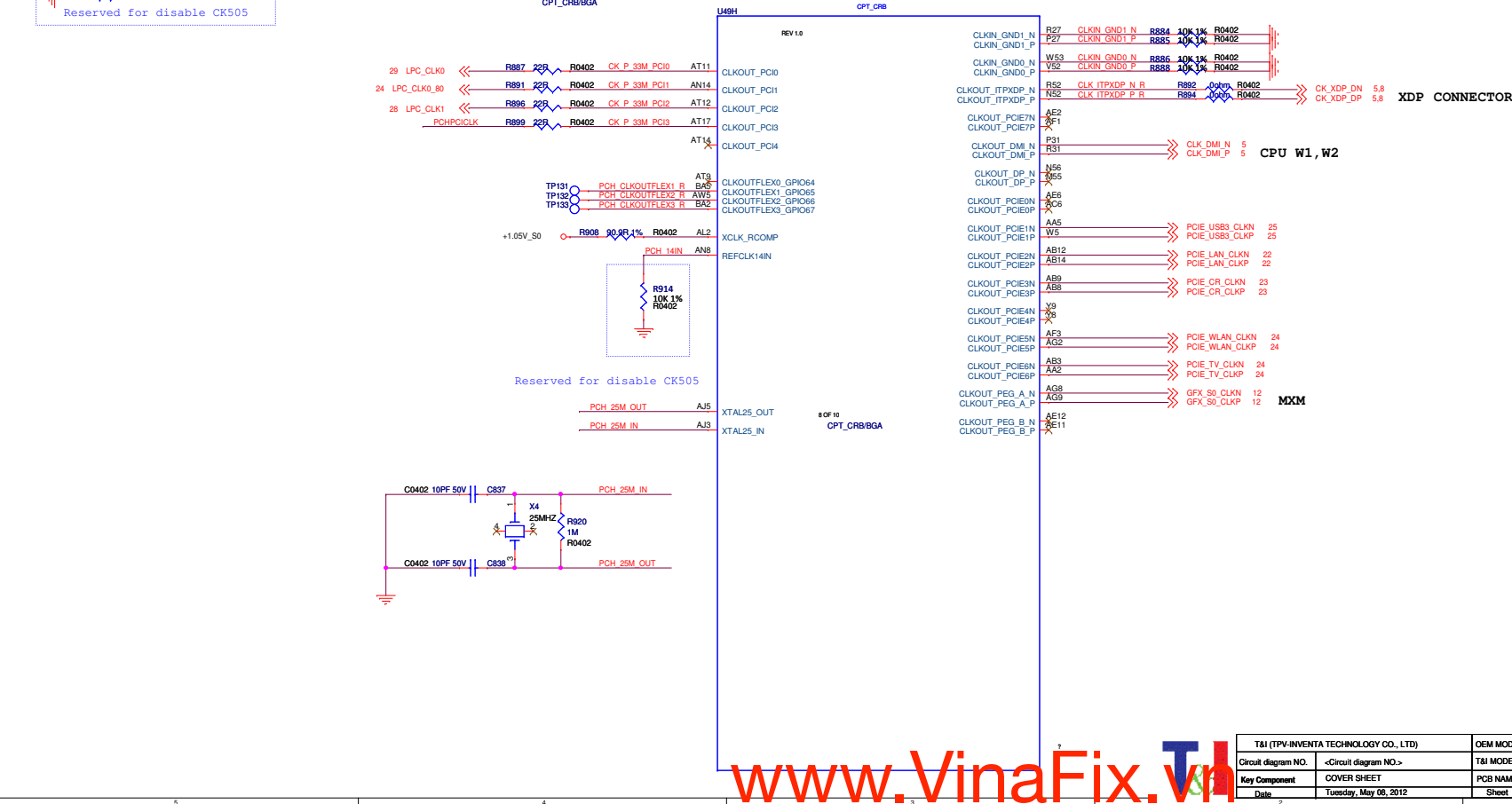
EDID



*PCH\_PCI*



## 8 XDP CONNECTOR



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lamybld		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXX0000000000		remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	14 of 43			

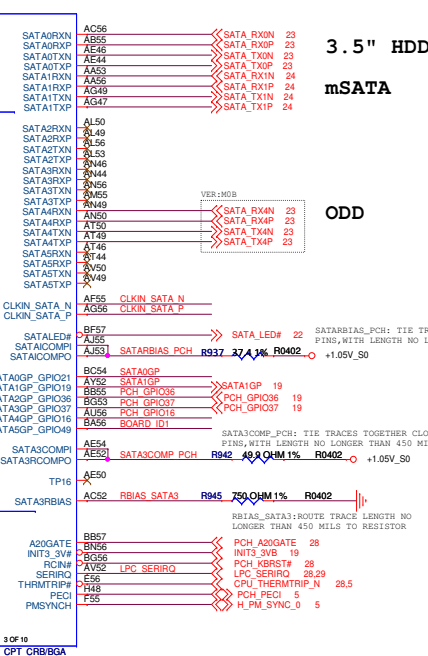
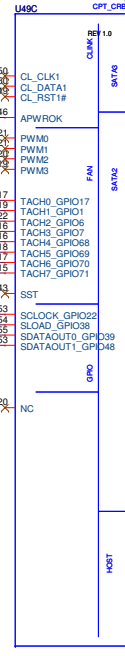
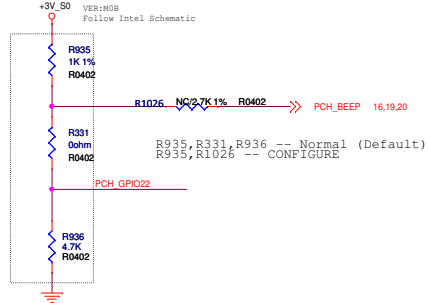


## PCH\_SATA

PCH\_MEPWROK:  
1) .V\_1P05\_ME  
2) .PCH\_SLP\_A

Not available in Mobile & Desktop

PCH\_CONFIG Recovery

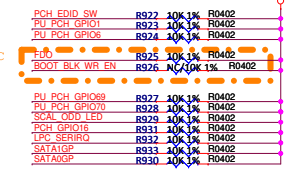


3.5" HDD

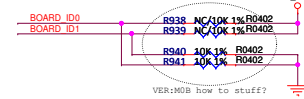
mSATA

ODD

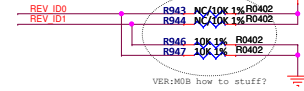
Pull HIGH for PCH



BOARD ID

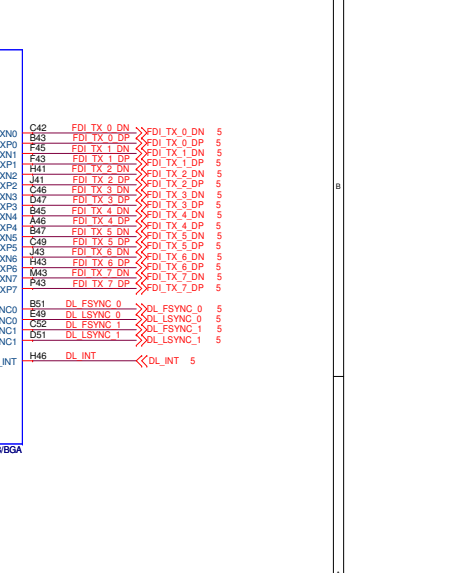
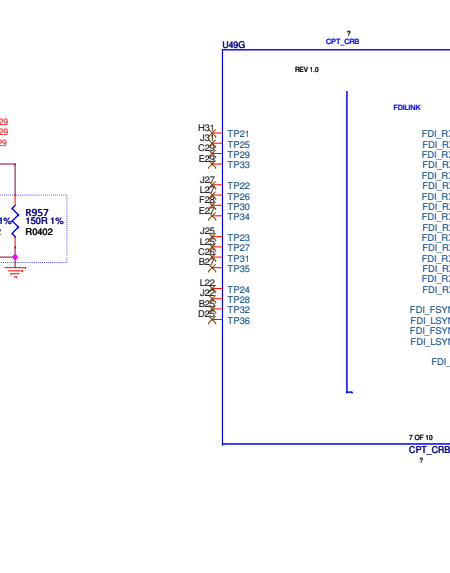
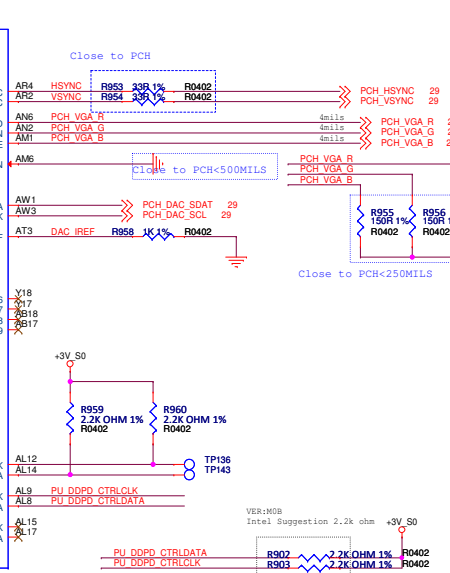
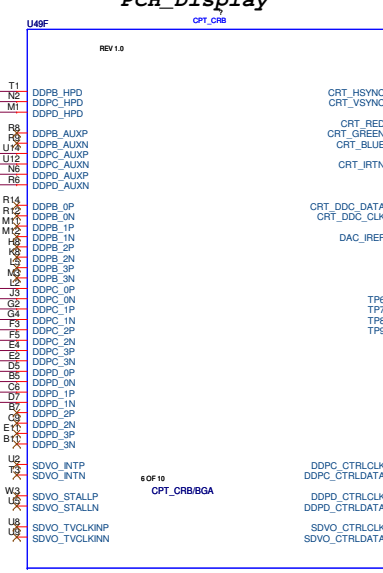
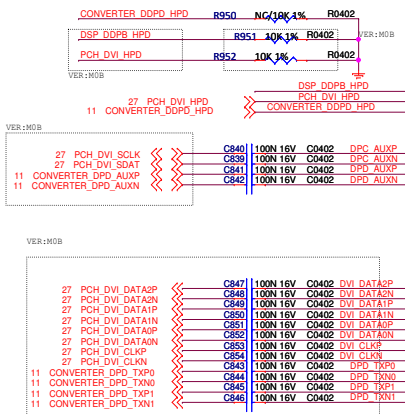


REV ID



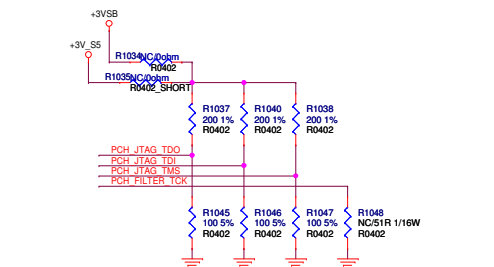
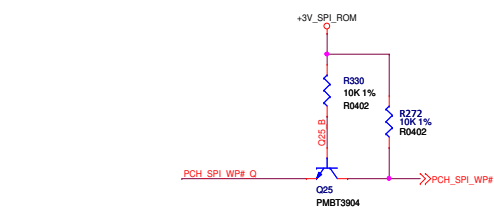
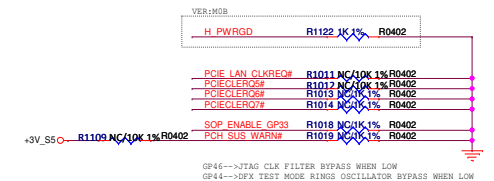
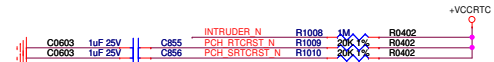
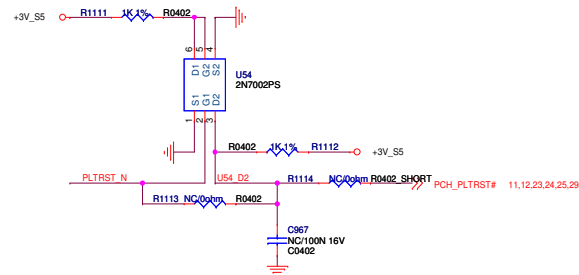
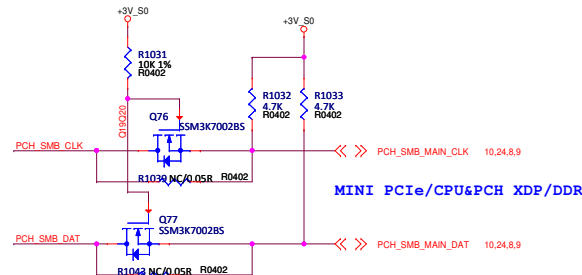
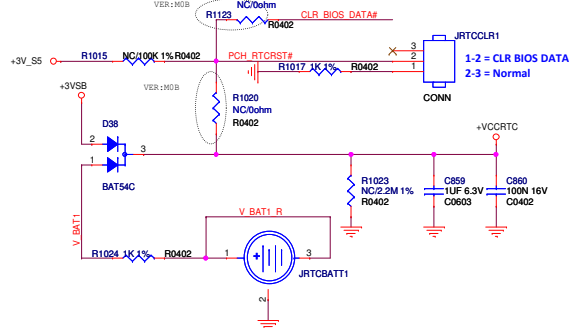
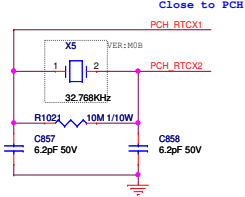
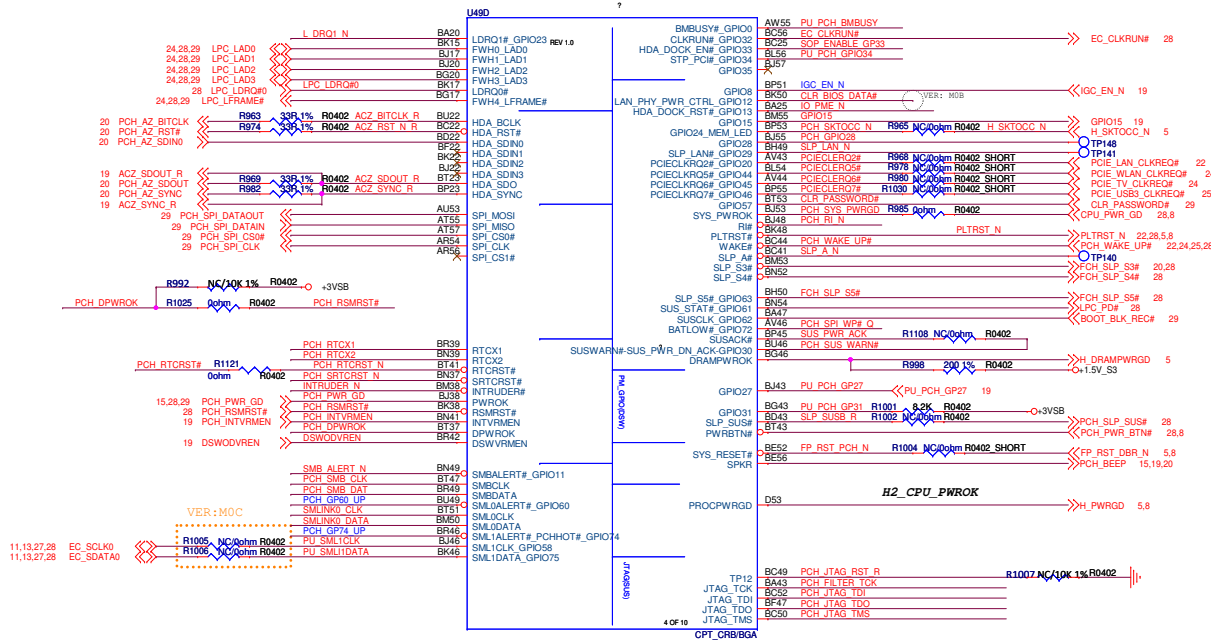
No VGA (pull down)

## PCH\_Display



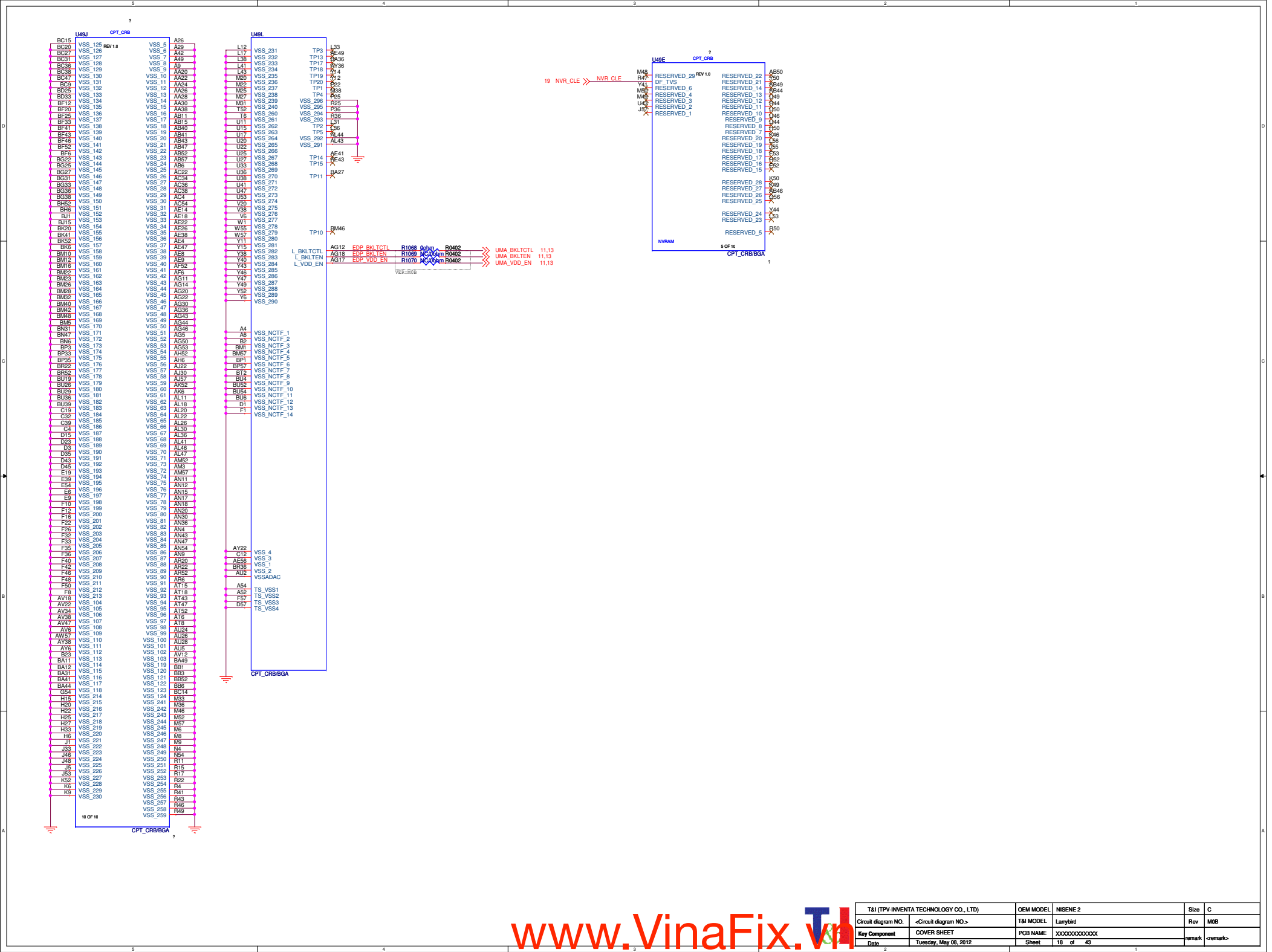
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	MOB
Date	Tuesday, May 06, 2012	Sheet	15 of 43	remark



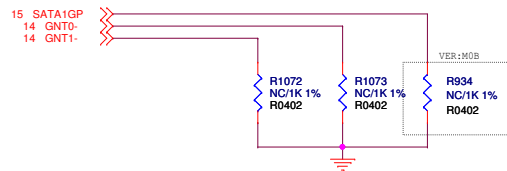


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
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Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		
Date	Tuesday, May 08, 2012	Sheet	16 of 43	remark	<remark>



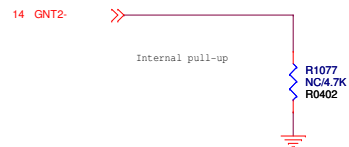


# CP REQUIRED STRAPS

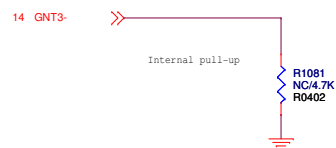


BOOT select straps

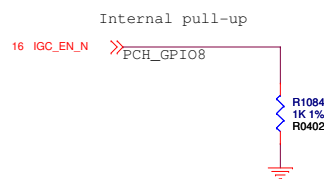
GNT1-	SATA1GP	Boot device
0	0	LPC
1	0	PCI
1	1	SPI(Default)



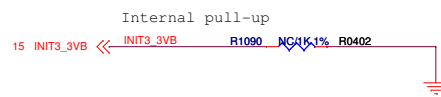
DMI AC/DC MODE  
0 : AC  
1 : DC \*



Topblock swap override when pull-low  
Signal has a weak internal pull-up

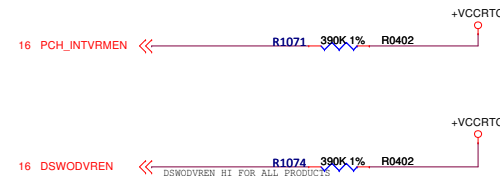


GPIO8  
0 : Integrated Clocking Enable (FCIM) \*  
1 : Buffer Through Mode Enable (BTM)



INT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*

1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.

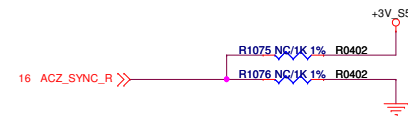


INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.



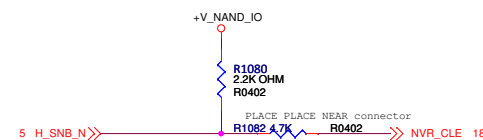
HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY

HDA\_SDO  
Disable ME in Manufacturing Mode  
when pull LOW ????

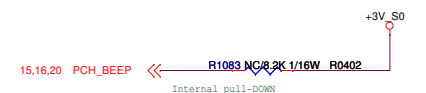
HDA\_SDO has internal pull down.  
Default should be connected to SDIN of codec, no pull up/down.  
To Disable ME need to have a jumper to pull high



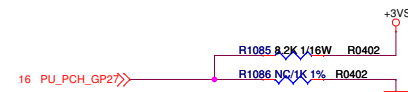
GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



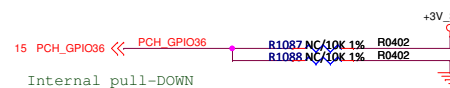
DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



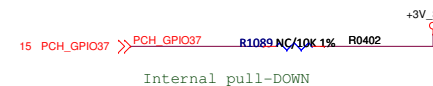
SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



In Deep Sleep Power Well.  
If not used, require a weak pull-up (8.2k-10k) to VccDSW3\_3



Cougar point EDS PAGE:93 This signal should not be pull high

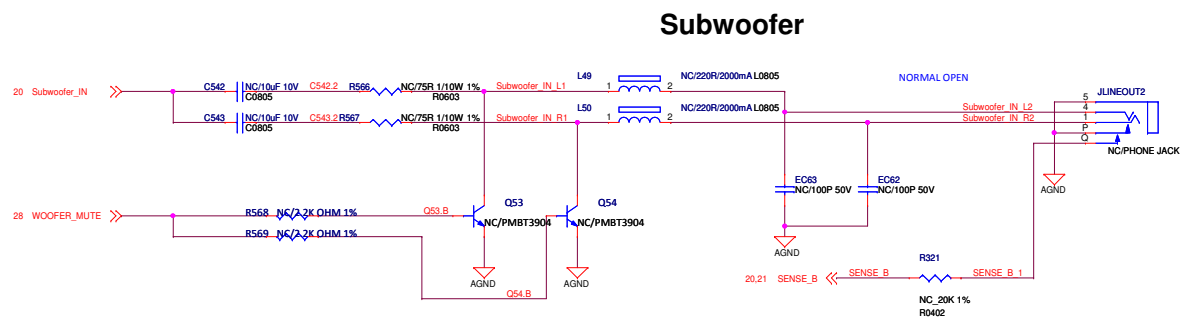
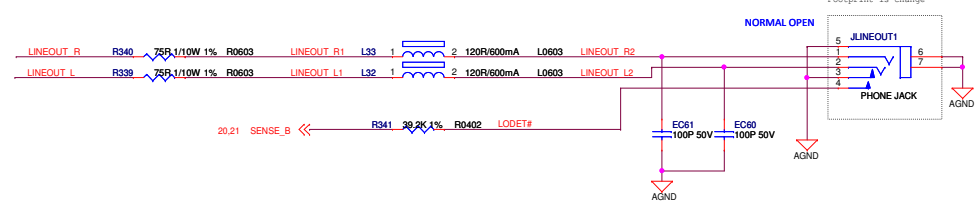
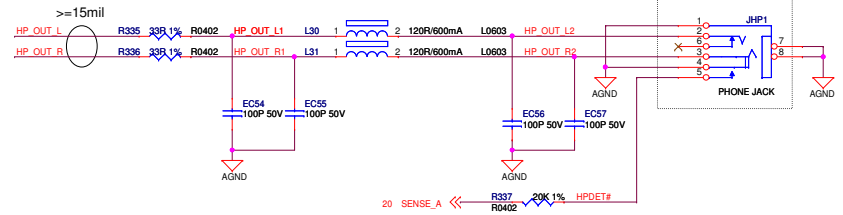
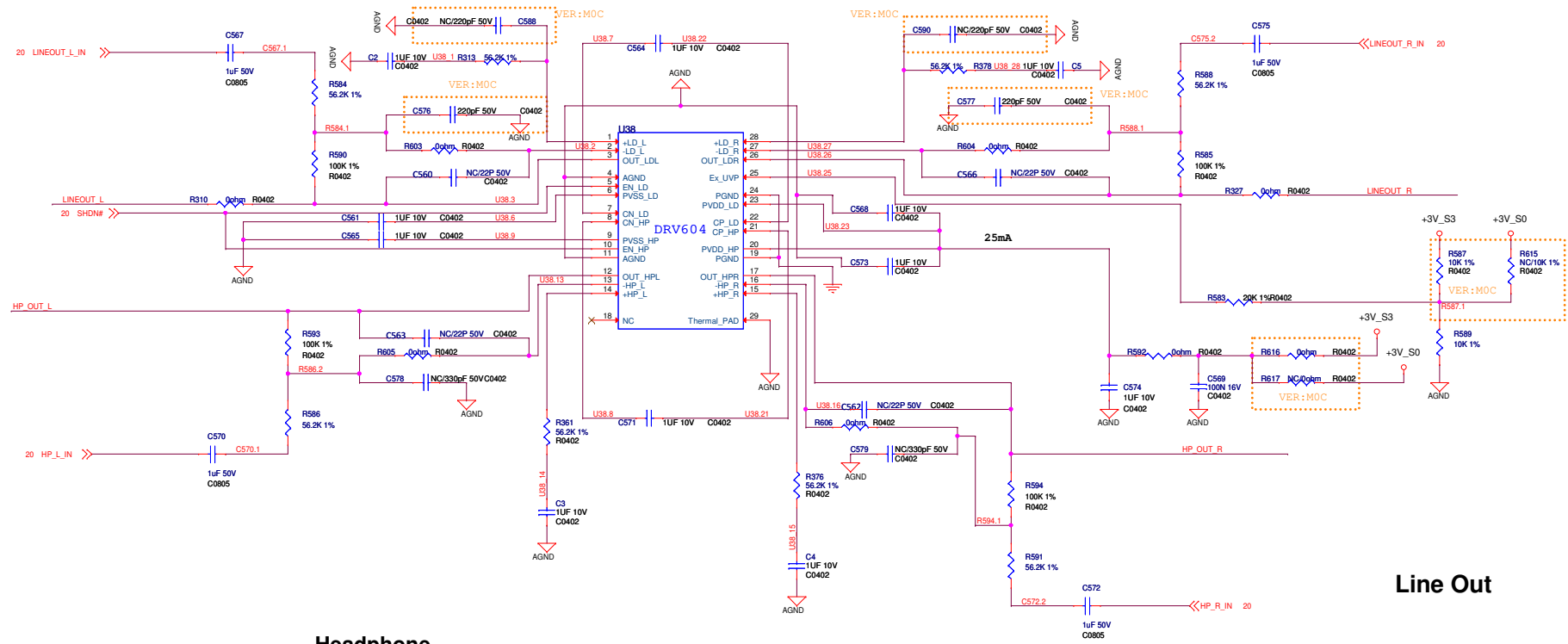


Cougar point EDS PAGE:93 This signal should not be pull high



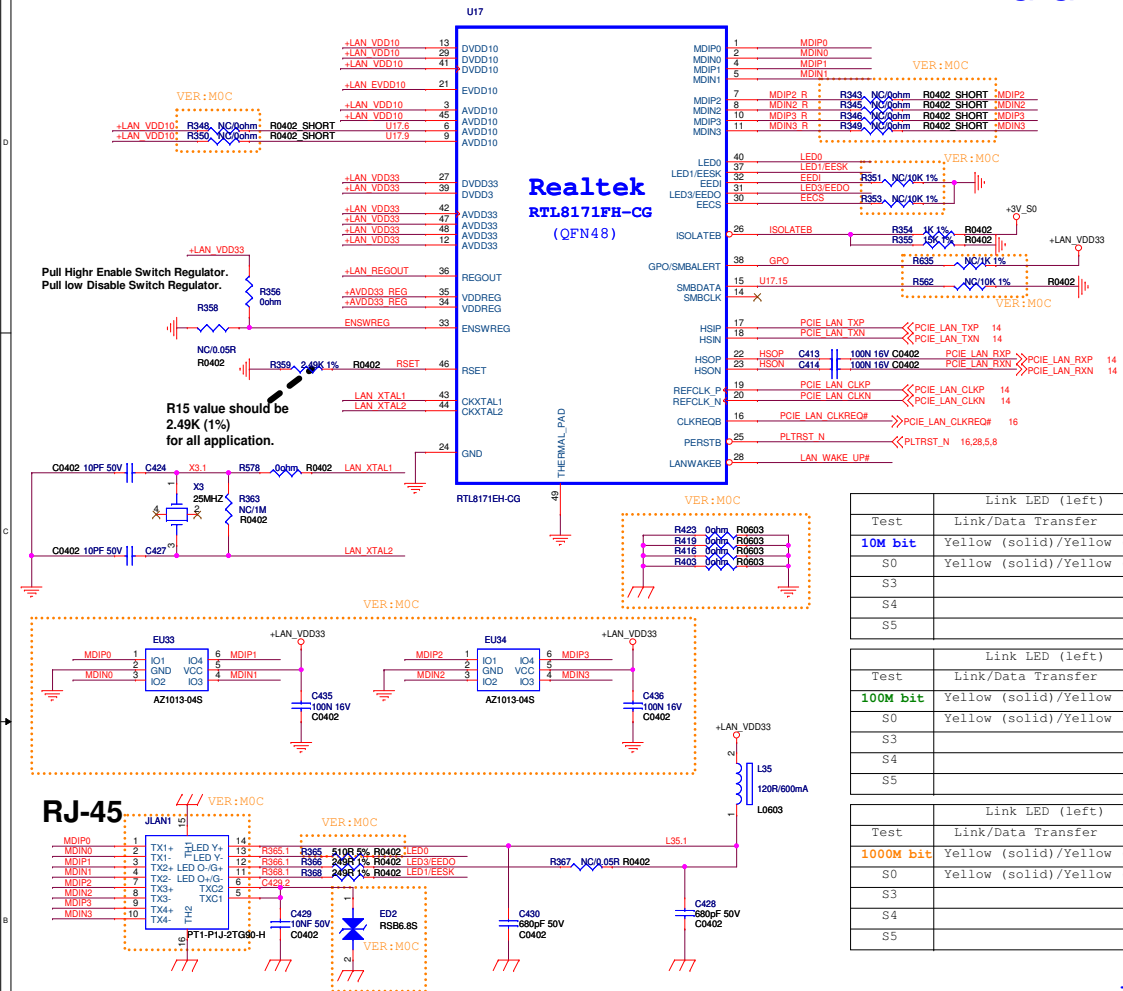
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	19 of 43	<remark>



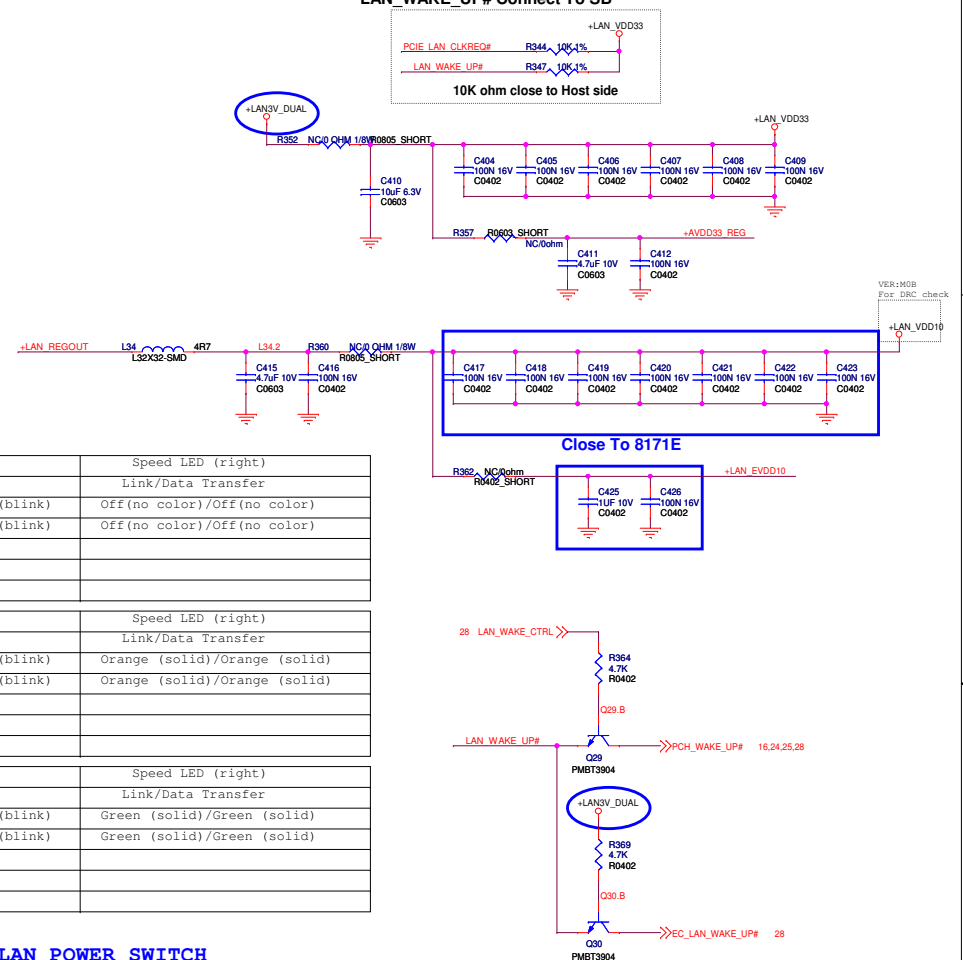


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lambybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	Remark
Date	Tuesday, May 06, 2012	Sheet	21 of 43	Remark

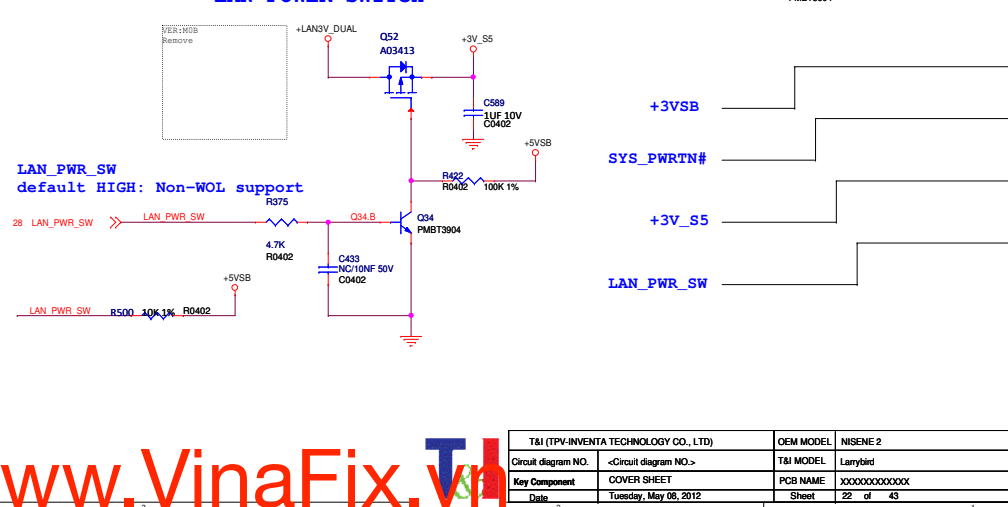
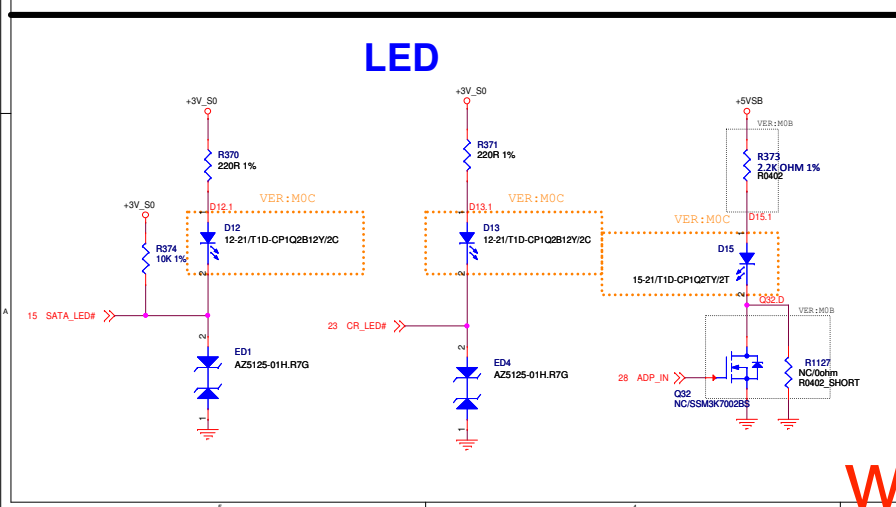
## GIGA LAN



PCIE\_LAN\_CLKREQ# Connect To SB  
LAN\_WAKE\_UP# Connect To SB



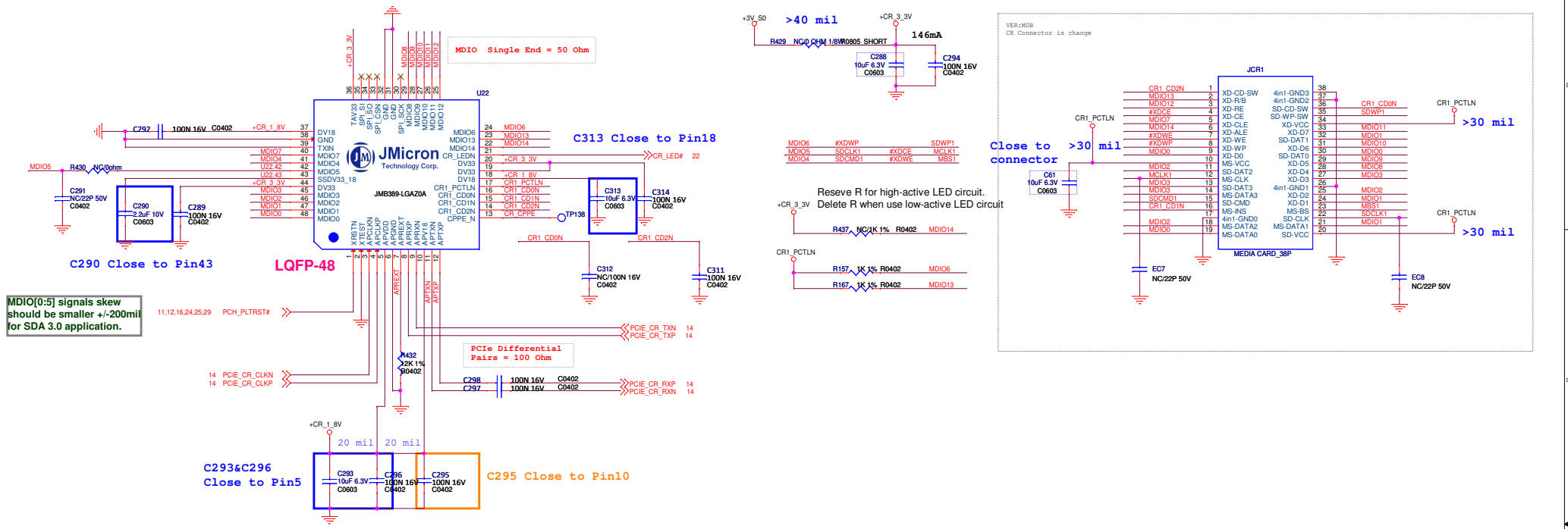
## LAN POWER SWITCH



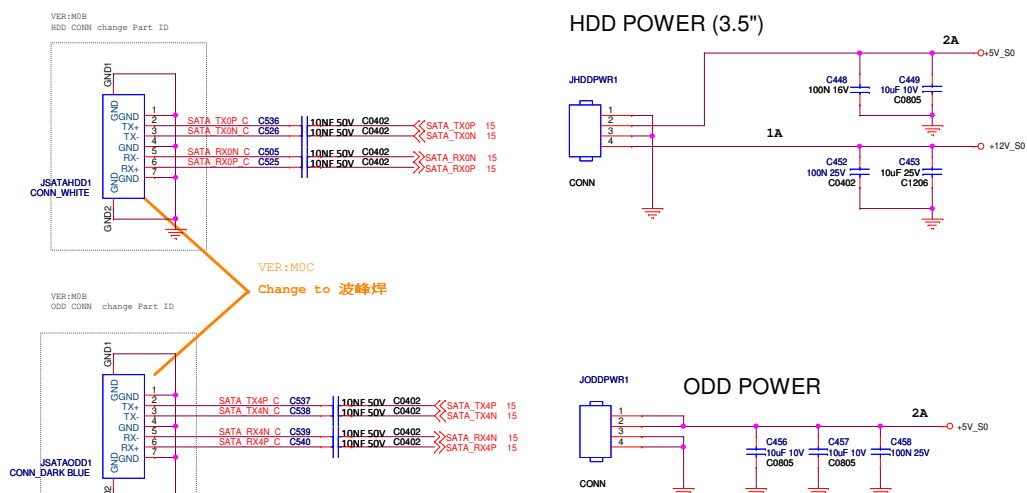
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lamybtd		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XX00000000000X			
Date	Tuesday, May 08, 2012	Sheet	22 of 43		remark	<remark>



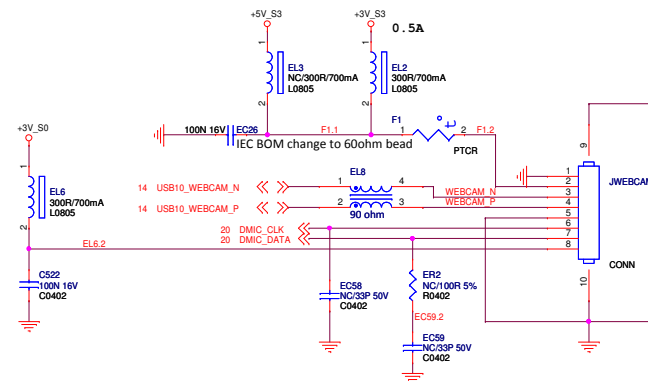
# Card Reader JMB389A



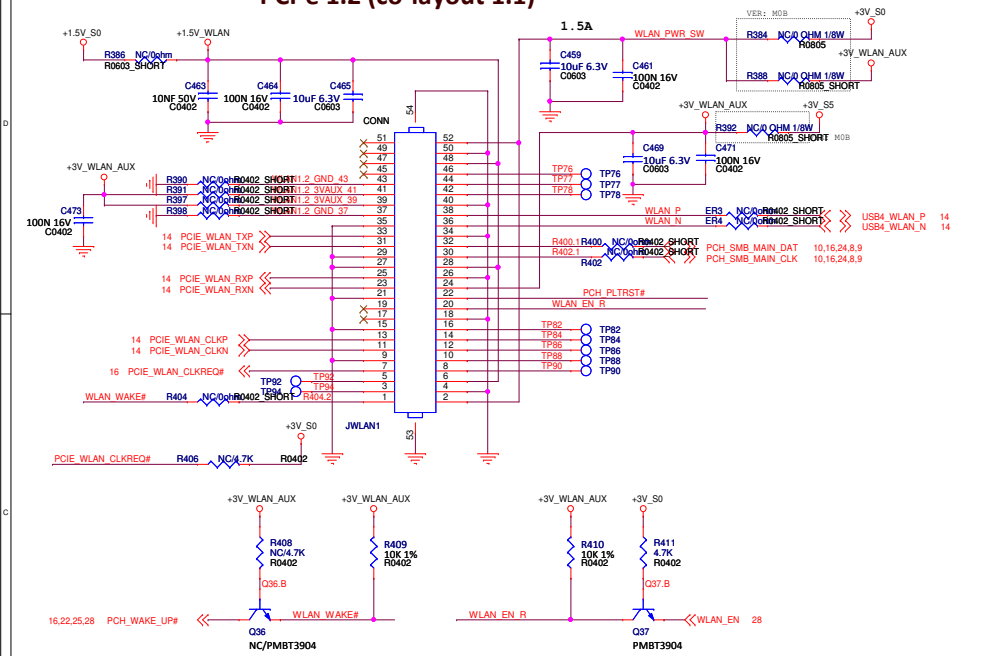
## HDD/ODD



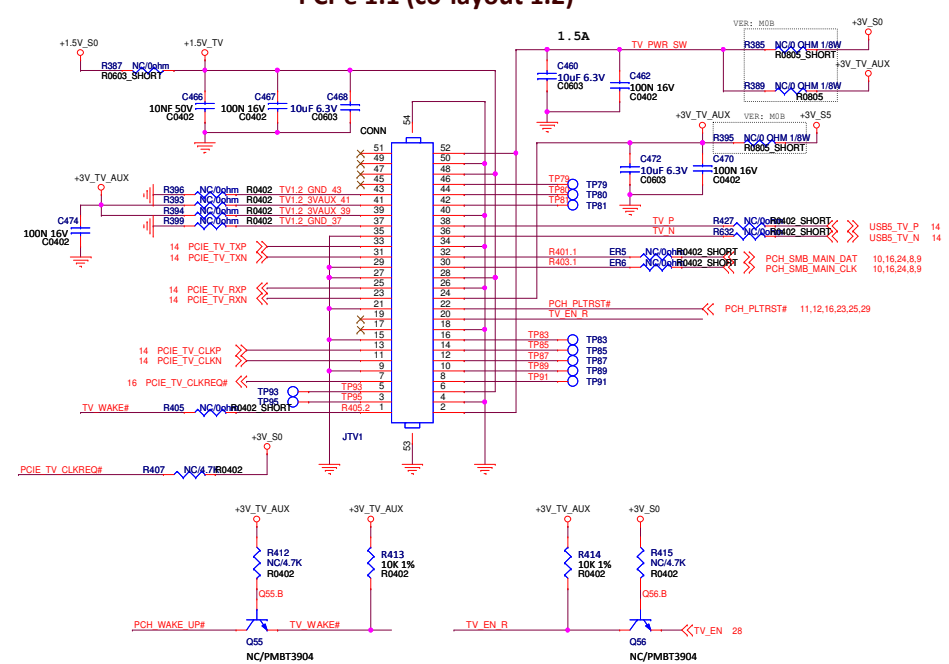
## WEB CAM



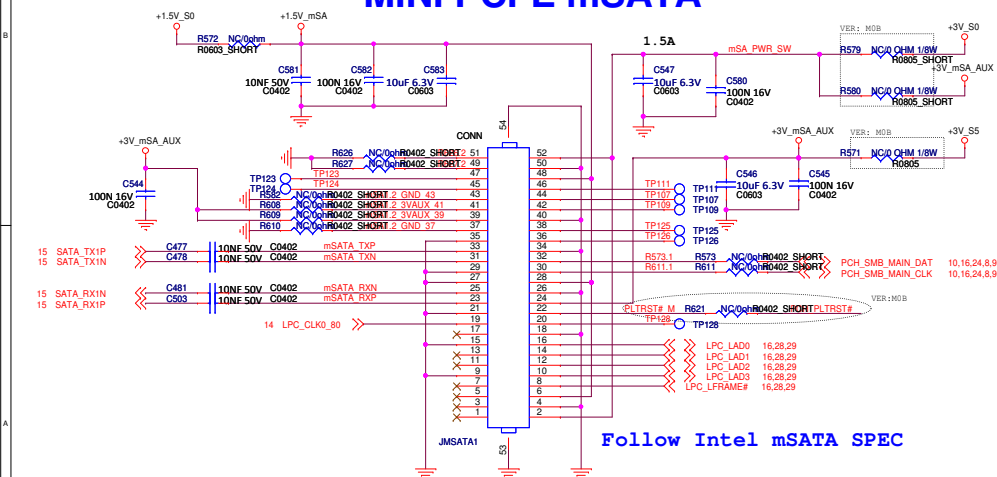
## MINI PCI-E WLAN & BT



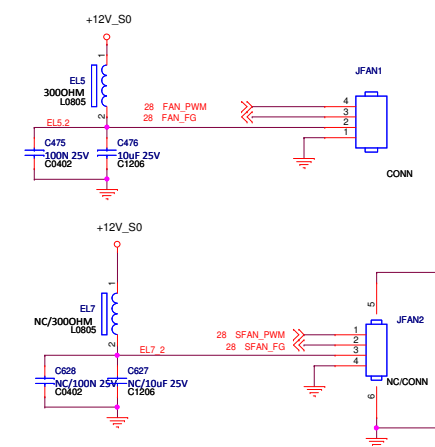
## MINI PCI-E TV CARD



## MINI PCI-E mSATA



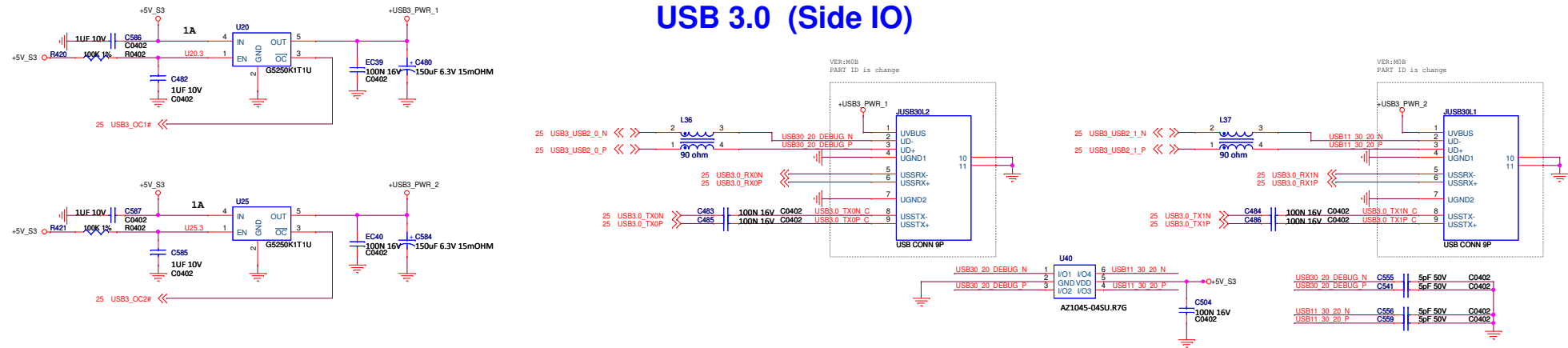
## CPU Linear FAN Control



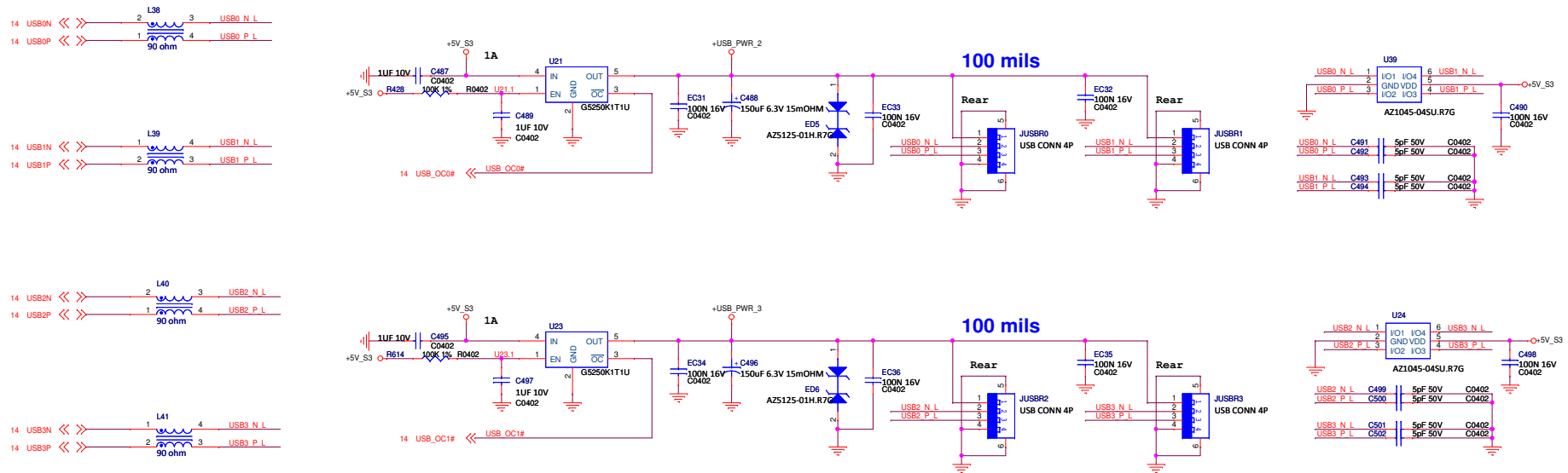
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	J00XXXXXXX0000XX			
Date	Tuesday, May 08, 2012	Sheet	24 of 43		remark	<remark>



## USB 3.0 (Side IO)



## USB 2.0 (Rear IO)

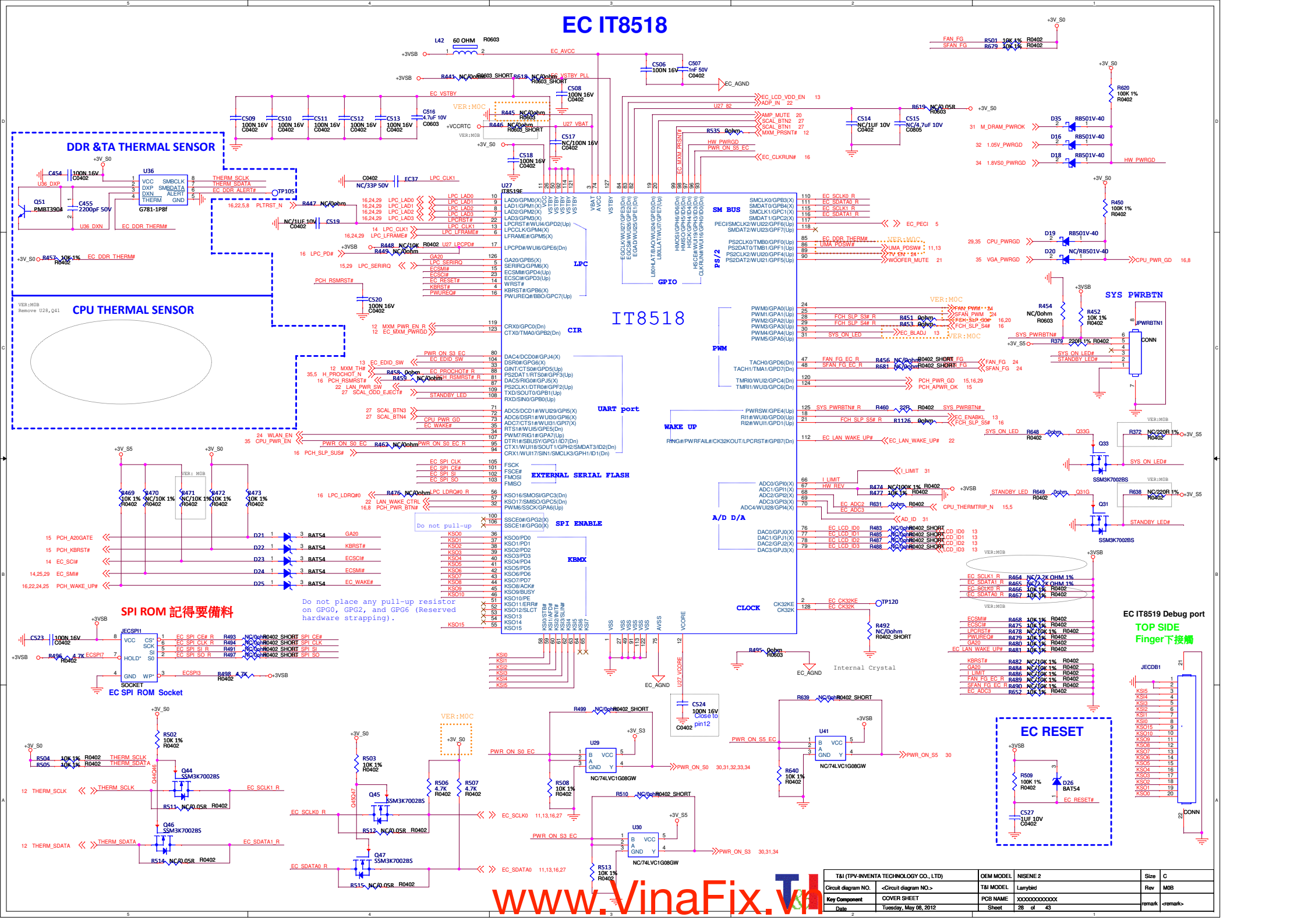


## USB 2.0 (Dongle)





# EC IT8518

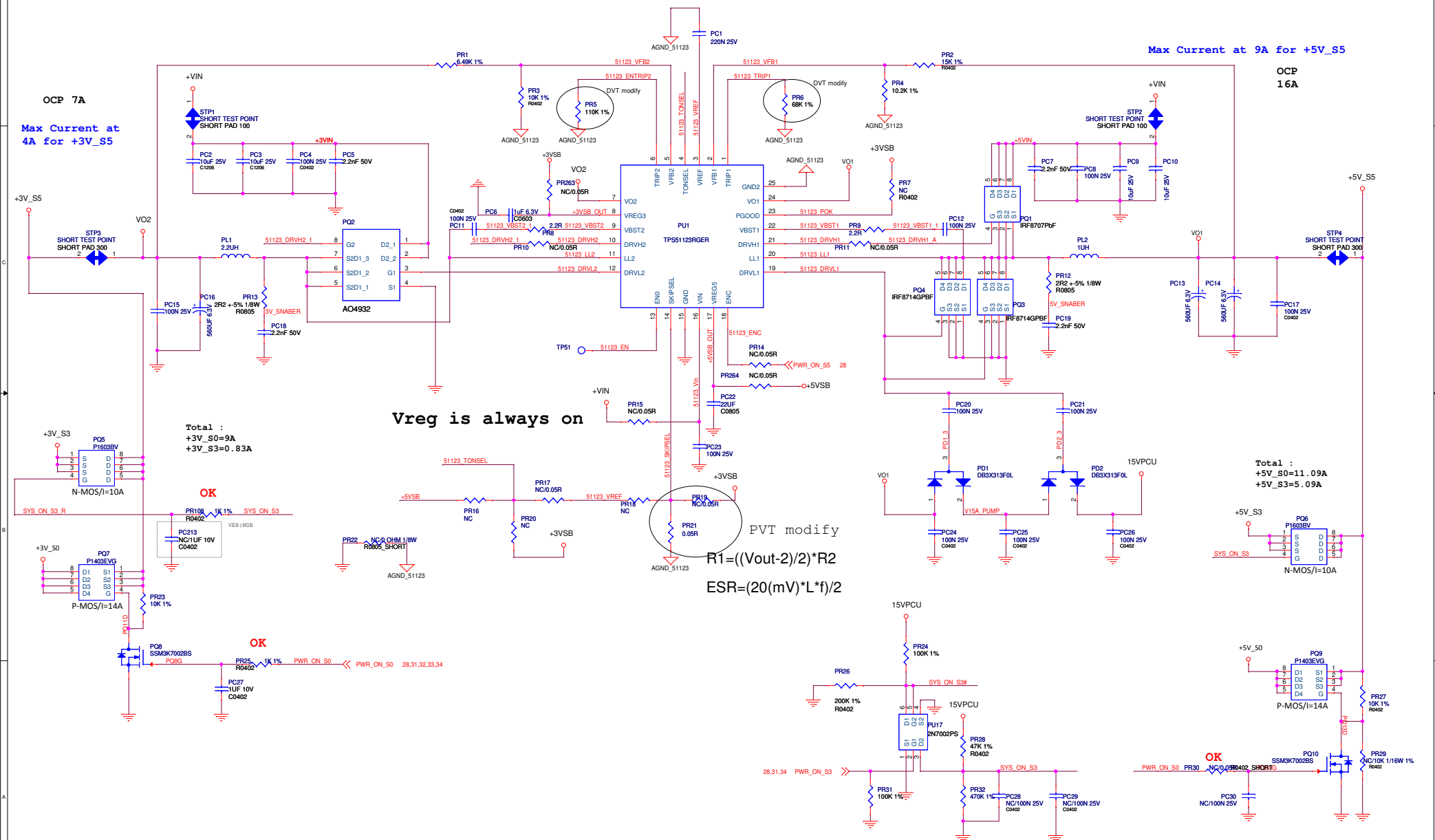


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	X0000000000	MB
Date	Tuesday, May 06, 2012	Sheet	28 of 43	remark





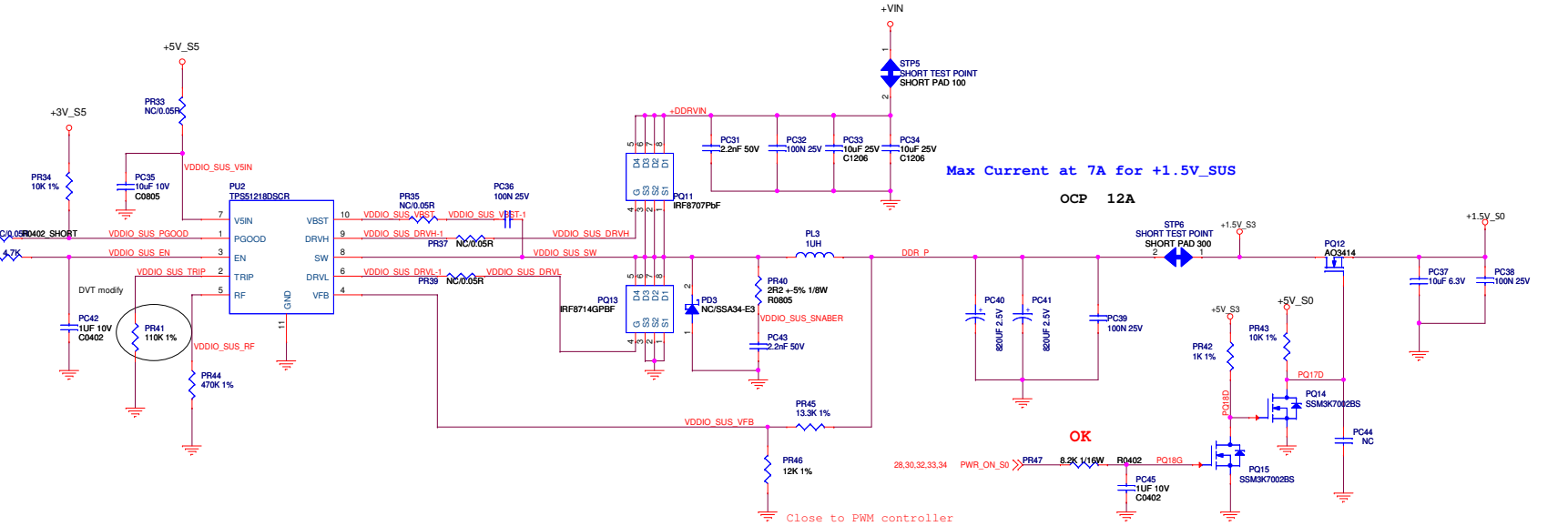
**SYSTEM +3V\_S5/+3V\_S3/+3V\_S0  
+5V\_S5/+5V\_S3/+5V\_S0**



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.		<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev	MOB
Key Component	COVER SHEET		PCB NAME	XXXXXXXXXXXXXX		
	Date	Tuesday, May 08, 2012	Sheet	30 of 43	remark	<remark>

# +1.5V\_SUS, MEM\_VTT, DC-IN

TOTAL POWER	I_LIMIT
0W	0V
10W	0.1282V
20W	0.2564V
30W	0.3846V
40W	0.5128V
50W	0.6410V
60W	0.7692V
70W	0.8974V
80W	1.0256V
90W	1.1538V
100W	1.2820V
110W	1.4102V
120W	1.5384V
130W	1.6666V
140W	1.7948V
150W	1.9230V
160W	2.0512V
170W	2.1794V
180W	2.3076V
190W	2.4359V
200W	2.5641V
210W	2.6923V
220W	2.8205V
230W	2.9487V

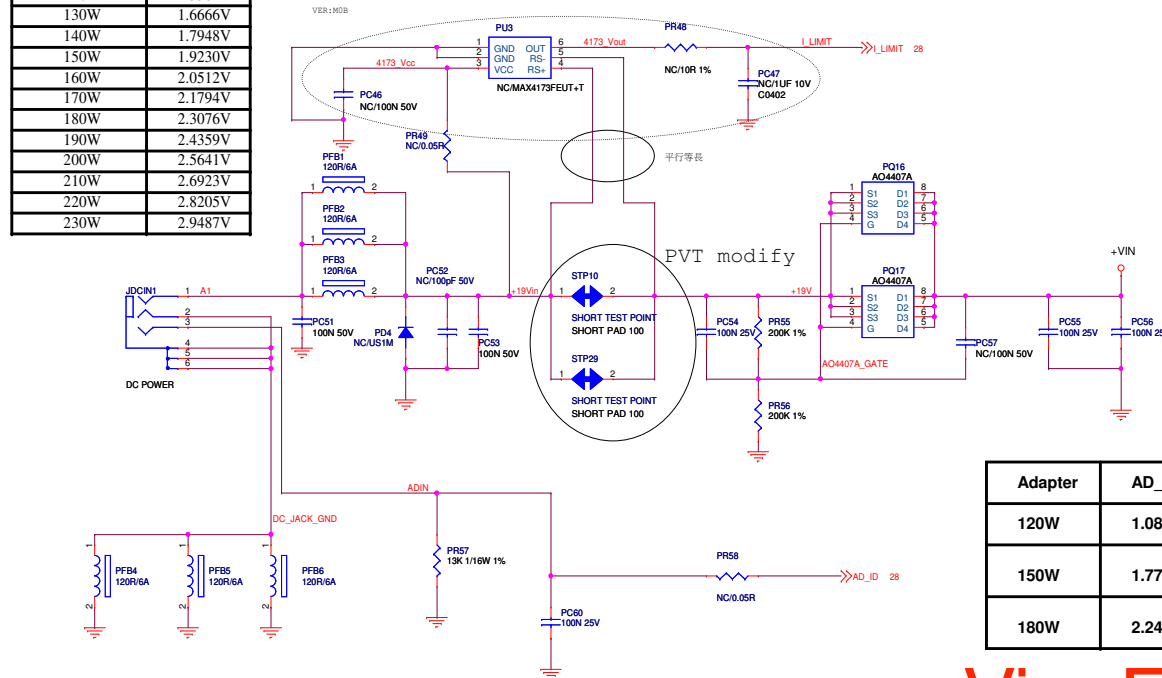
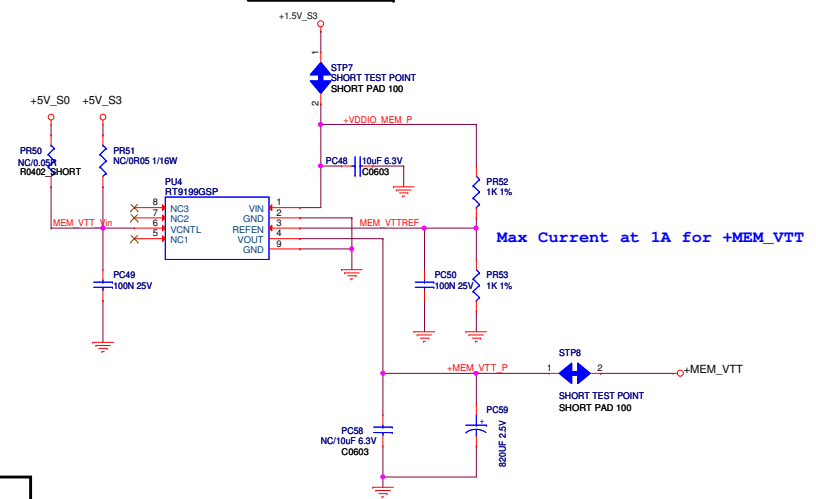


Close to PWM controller

$$V_{out} = 0.704V * (R1 + R2) / R2$$

$$ESR = L * f / 70$$

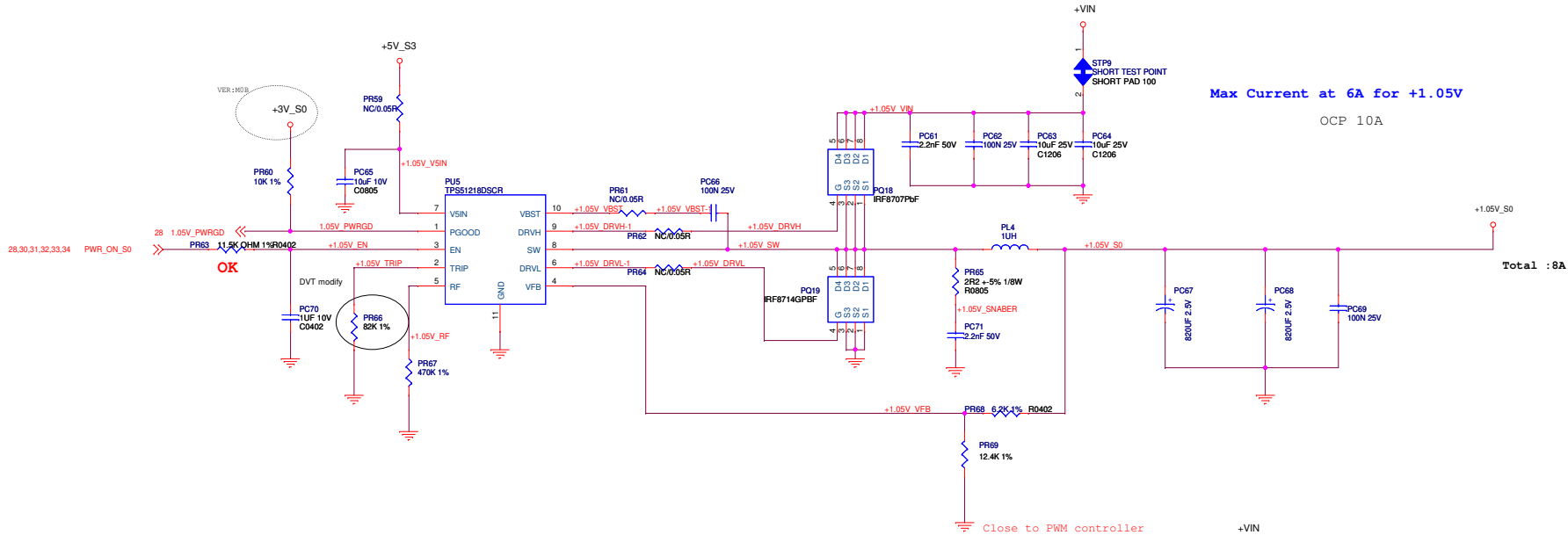
## MEM\_VTT Power



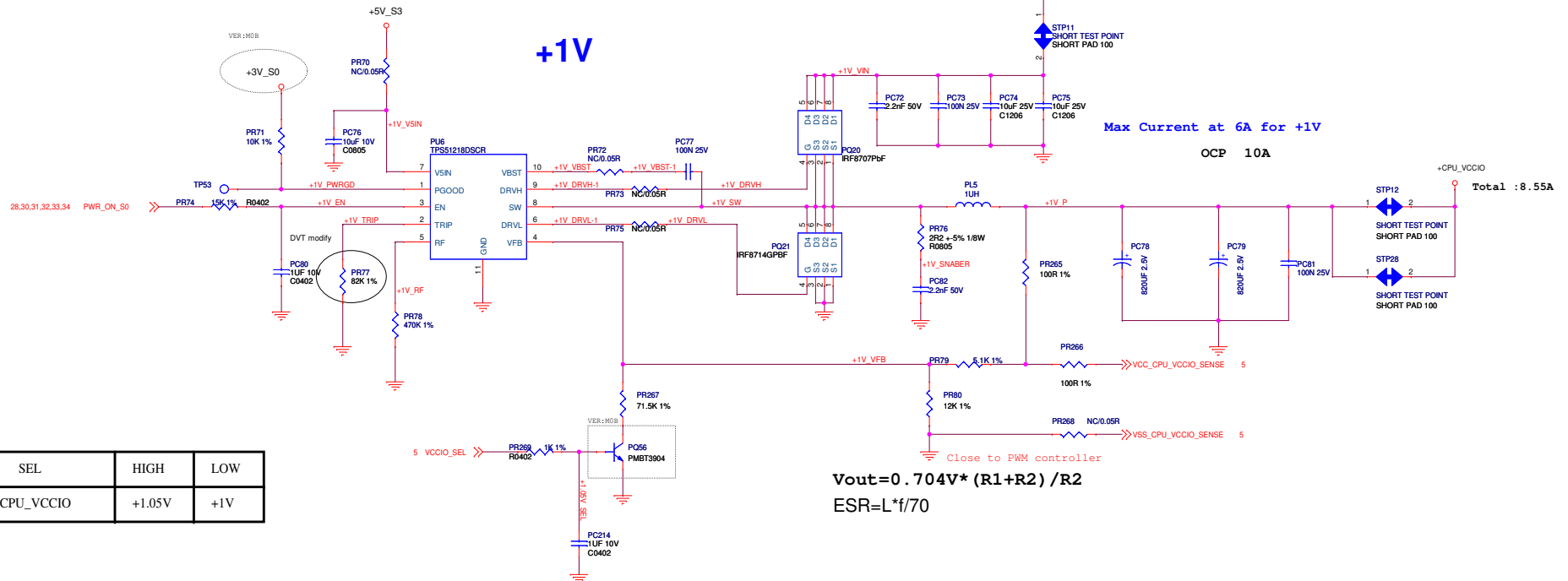
Adapter	AD_ID
120W	1.08V
150W	1.77V
180W	2.24V

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NIENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	MOB
Date	Tuesday, May 06, 2012	Sheet	31 of 43	remark

**+1.05V**

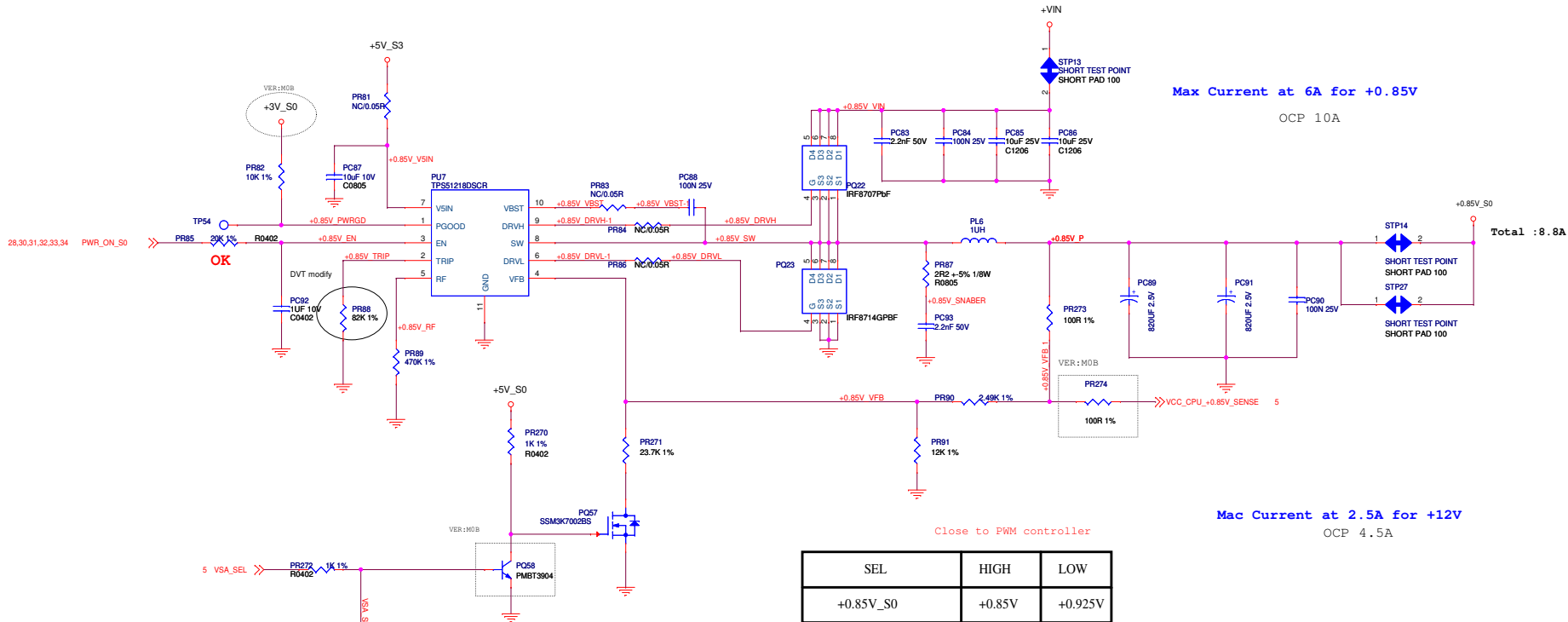


**+1V**



SEL	HIGH	LOW
+CPU_VCCIO	+1.05V	+1V

+0.85V



Max Current at 6A for +0.85V

OCP 10A

Total : 8.8A

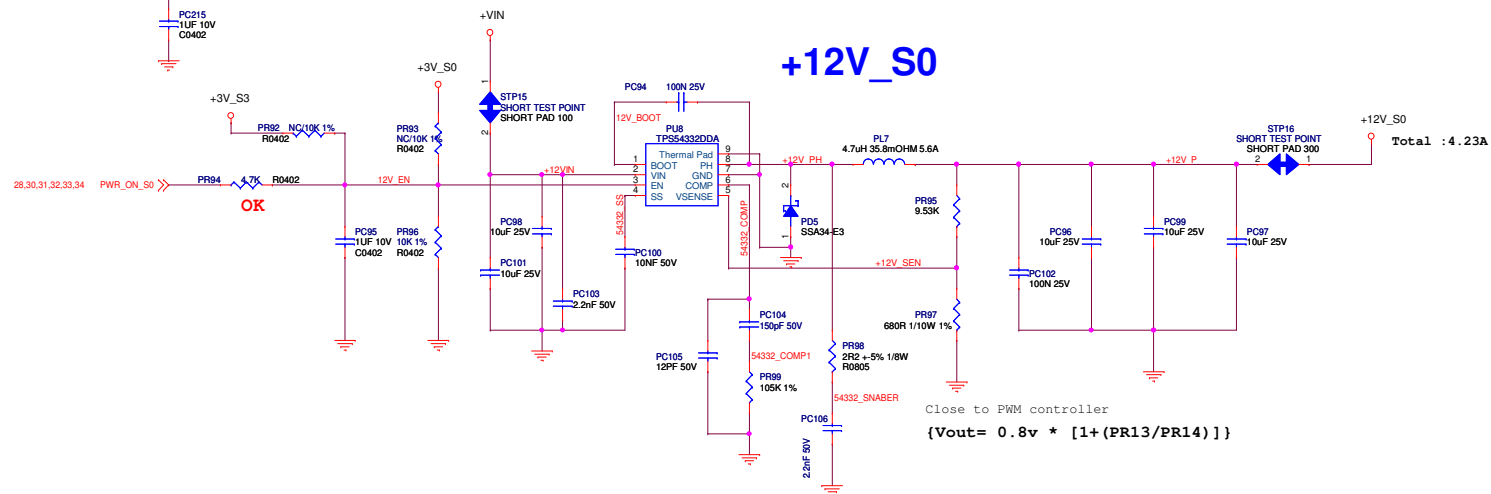
Close to PWM controller

Mac Current at 2.5A for +12V

OCP 4.5A

SEL	HIGH	LOW
+0.85V_S0	+0.85V	+0.925V

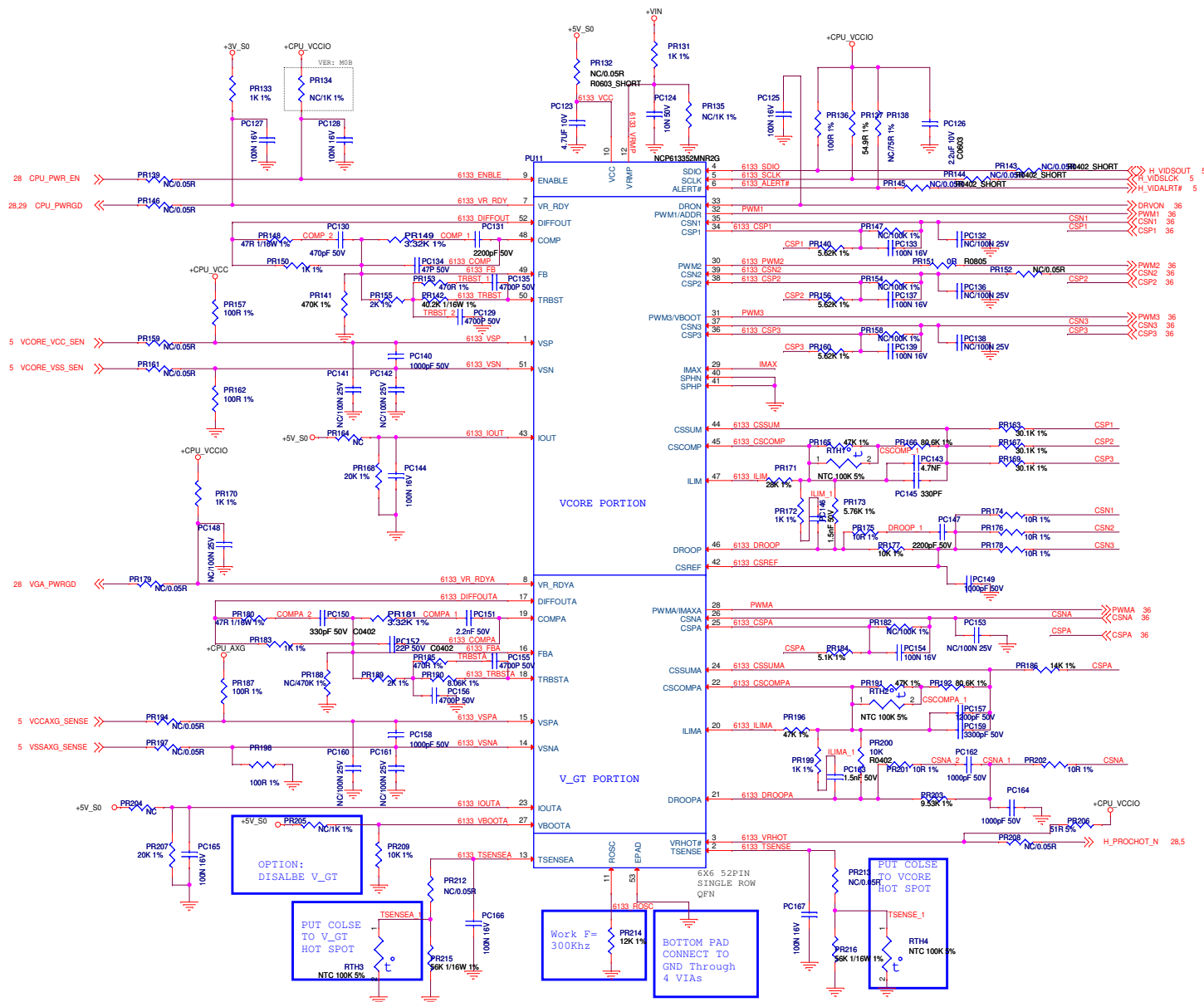
+12V\_S0



Close to PWM controller

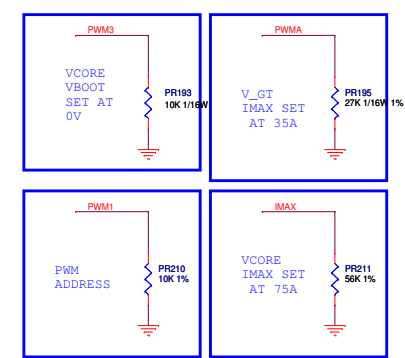
{Vout= 0.8v \* [1+(PR13/PR14)]}

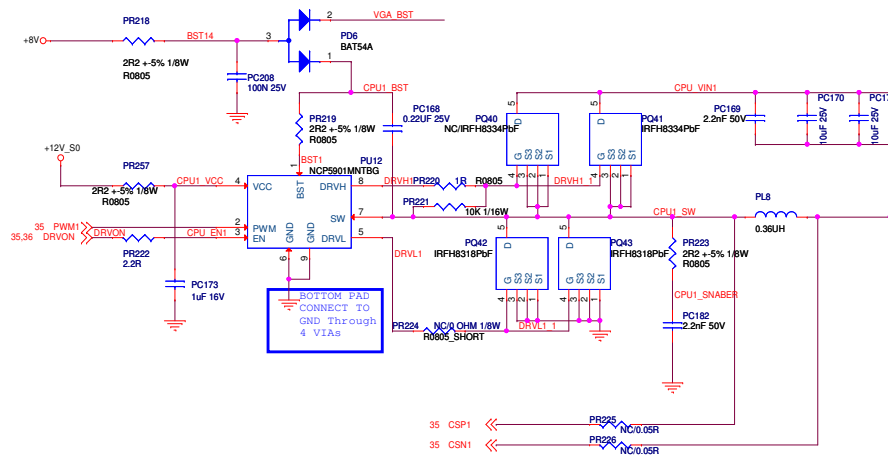




PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR Vcore RAIL	SVID ADDRESS FOR Vgt RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

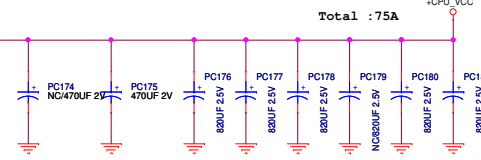
BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V
VCC	SHUTDOWN





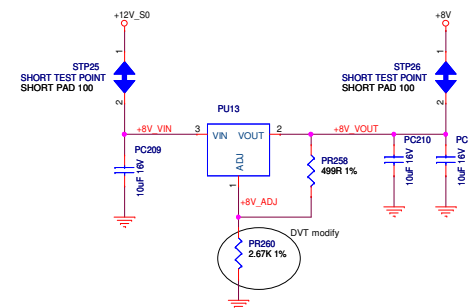
Max Current at  
60A for +CPU\_CORE

OCB  
90A



+8V

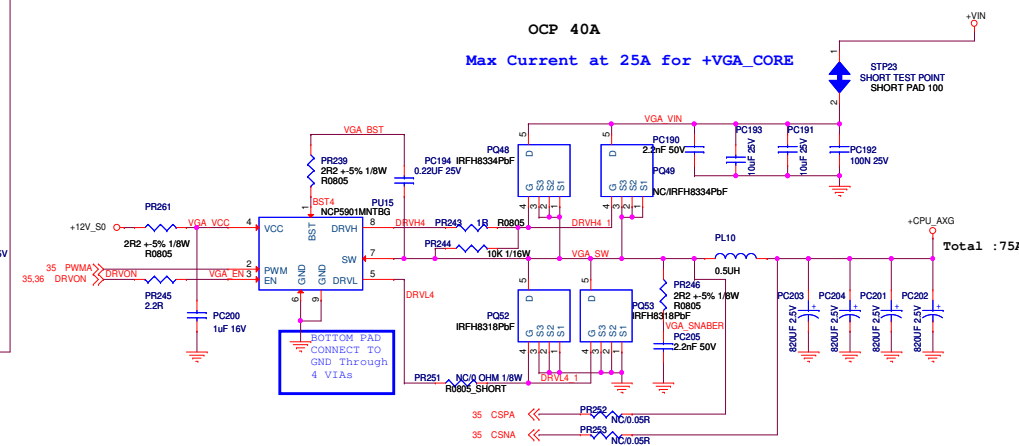
Max Current at 0.5A for +8V



$$VO = VREF \left( 1 + \frac{R2}{R1} \right) + IADJ \times R2$$

OCB 40A

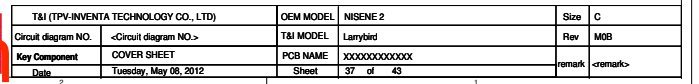
Max Current at 25A for +VGA\_CORE



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
COVER SHEET		PCB NAME	X00000000000	MOB
Date	Tuesday, May 06, 2012	Sheet	36 of 43	remark



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PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO0	AW55	I/O	3.3 V	Core	GPI	BMBUSY#	PU_PCH_BMBUSY
GPIO1	BR19	I/O	3.3 V	Core	GPI	TACH1	PU_PCH_GPIO1
GPIO2	BN9	I/OD	5 V	Core	GPI	PIRQE#	PIRQE_N
GPIO3	AV9	I/OD	5 V	Core	GPI	PIRQF#	PIRQF_N
GPIO4	BT15	I/OD	5 V	Core	GPI	PIRQG#	PIRQG_N
GPIO5	BR4	I/OD	5 V	Core	GPI	PIRQH#	PIRQH_N
GPIO6	BA22	I/O	3.3 V	Core	GPI	TACH2	PU_PCH_GPIO6
GPIO7	BR16	I/O	3.3 V	Core	GPI	TACH3	FDO
GPIO8	BP51	I/O	3.3 V	Suspend	GPO	NA	IGC_EN_N
GPIO9	BJ41	I/O	3.3 V	Suspend	Native	OC5#	USB_OC5#
GPIO10	BT45	I/O	3.3 V	Suspend	Native	OC6#	EC_SCI#
GPIO11	BN49	I/O	3.3 V	Suspend	Native	SMBALERT#	SMB_ALERT_N
GPIO12	BK50	I/O	3.3 V	Suspend	Native	LAN_PHY_PWR_CTRL	CLR_BIOS_DATA#
GPIO13	BA25	I/O	3.3 V	Suspend	GPI	HDA_DOCK_RST#	IO_PME_N
GPIO14	BM45	I/O	3.3 V	Suspend	Native	OC7#	EC_SMI#
GPIO15	BM55	I/O	3.3 V	Suspend	GPO	GPIO15	GPIO15
GPIO16	AU56	I/O	3.3 V	Core	GPI	SATA4GP	PCH_GPIO16
GPIO17	BT17	I/O	3.3 V	Core	GPI	TACH0	PCH_EDID_SW
GPIO18	Mobile Only	I/O	3.3 V	Core	Native	NA	NA
GPIO19	AY52	I/O	3.3 V	Core	GPI	SATA1GP	SATA1GP
GPIO20	AV43	I/O	3.3 V	Core	Native	PCIECLKRQ2#	PCIE_LAN_CLKREQ#
GPIO21	BC54	I/O	3.3 V	Core	GPI	SATA0GP	SATA0GP
GPIO22	BA53	I/O	3.3 V	Core	GPI	SCLOCK	PCH_GPIO22
GPIO23	BA20	I/O	3.3 V	Core	Native	LDRQ1#	L_DRQ1_N
GPIO24	BP53	I/O	3.3 V	Suspend	GPO	MEM_LED	H_SKTOCC_N
GPIO25	Mobile Only	I/O	3.3 V	Suspend	Native	NA	NA
GPIO26	Mobile Only	I/O	3.3 V	Suspend	Native	NA	NA
GPIO27	BJ43	I/O	3.3 V	DSW	GPI	GPIO27	PU_PCH_GP27
GPIO28	BJ55	I/O	3.3 V	Suspend	GPO	GPIO28	SLP_LAN_N
GPIO29	BH49	I/O	3.3 V	Suspend	GPI	SLP_LAN#	PCIE_LAN_CLKREQ#
GPIO30	BU46	I/O	3.3 V	Suspend	Native	SUSWARN#	PCH_SUS_WARN#
GPIO31	BG43	I/O	3.3 V	DSW	GPI	GPIO31	PU_PCH_GP31
GPIO32	BC56	I/O	3.3 V	Core	GPO	CLKRUN#	EC_CLKRUN#

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	38	of	43	

## PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO33	BC25	I/O	3.3 V	Core	GPO	NA	SOP_ENABLE_GP33
GPIO34	BL56	I/O	3.3 V	Core	GPI	STP_PCI#	PU_PCH_GPIO34
GPIO35	BJ57	I/O	3.3 V	Core	GPO	NMI#	No connected
GPIO36	BB55	I/O	3.3 V	Core	GPI	SATA2GP	PCH_GPIO36
GPIO37	BG53	I/O	3.3 V	Core	GPI	SATA3GP	PCH_GPIO37
GPIO38	BE54	I/O	3.3 V	Core	GPI	SLOAD	BOARD_ID0
GPIO39	BF55	I/O	3.3 V	Core	GPI	SDATAOUT0	REV_ID0
GPIO40	BD41	I/O	3.3 V	Suspend	Native	OC1#	USB_OC1#
GPIO41	BG41	I/O	3.3 V	Suspend	Native	OC2#	USB_OC2#
GPIO42	BK43	I/O	3.3 V	Suspend	Native	OC3#	USB_OC3#
GPIO43	BP43	I/O	3.3 V	Suspend	Native	OC4#	USB_OC4#
GPIO44	BL54	I/O	3.3 V	Suspend	Native	PCIECLKRQ5#	PCIE_WLAN_CLKREQ#
GPIO45	AV44	I/O	3.3 V	Suspend	Native	PCIECLKRQ6#	PCIE_TV_CLKREQ#
GPIO46	BP55	I/O	3.3 V	Suspend	Native	PCIECLKRQ7#	PCIE_USB3_CLKREQ#
GPIO47	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO48	AW53	I/O	3.3 V	Core	GPI	SDATAOUT1	REV_ID1
GPIO49	BA56	I/O	3.3 V	Core	GPI	SATA5GP	BOARD_ID1
GPIO50	BT5	I/O	5.0 V	Core	Native	REQ1#	REQ1_N
GPIO51	AV8	I/O	3.3 V	Core	Native	GNT1#	GNT1-
GPIO52	BK8	I/O	5.0 V	Core	Native	REQ2#	REQ2_N
GPIO53	BU12	I/O	3.3 V	Core	Native	GNT2#	GNT2-
GPIO54	AV11	I/O	5.0 V	Core	Native	REQ3#	REQ3_N
GPIO55	BE2	I/O	3.3 V	Core	Native	GNT3#	GNT3-
GPIO56	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO57	BT53	I/O	3.3 V	Suspend	GPI	NA	CLR_PASSWORD#
GPIO58	BJ46	I/O	3.3 V	Suspend	Native	SML1CLK	EC_SCLK0
GPIO59	BM43	I/O	3.3 V	Suspend	Native	OC0#	USB_OC0#
GPIO60	BU49	I/O	3.3 V	Suspend	Native	SML0ALERT#	PCH_GP60_UP
GPIO61	BN54	I/O	3.3 V	Suspend	Native	SUS_STAT#	LPC_PD#
GPIO62	BA47	I/O	3.3 V	Suspend	Native	SUSCLK	BOOT_BLK_REC#
GPIO63	BH50	I/O	3.3 V	Suspend	Native	SLP_S5#	FCH_SLP_S5#
GPIO64	AT9	I/O	3.3 V	Core	Native	CLKOUTFLEX0	No connected
GPIO65	BA5	I/O	3.3 V	Core	Native	CLKOUTFLEX1	Test Point

PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO66	AW5	I/O	3.3 V	Core	Native	CLKOUTFLEX2	Test Point
GPIO67	BA2	I/O	3.3 V	Core	Native	CLKOUTFLEX3	Test Point
GPIO68	BU16	I/O	3.3 V	Core	GPI	TACH4	BOOT_BLK_WR_EN
GPIO69	BM18	I/O	3.3 V	Core	GPI	TACH5	PU_PCH_GPIO69
GPIO70	BN17	I/O	3.3 V	Core	Native	TACH6	PU_PCH_GPIO70
GPIO71	BP15	I/O	3.3 V	Core	Native	TACH7	SCAL_ODD_LED
GPIO72	AV46	I/O	3.3 V	Suspend	Native	BATLOW#	PCH_SPI_WP#_Q
GPIO73	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO74	BR46	I/O	3.3 V	Suspend	Native	SML1ALERT# or PCHHOT#	PCH_GP74_UP
GPIO75	BK46	I/O	3.3 V	Suspend	Native	SML1DATA	PU_SMLI1DATA

Schematic Modify History

MOA to MOB

Page-5 ,Add C933 C994,Power suggesstion  
R687 is change PART ID  
Add net "VCC\_CPU\_+0.85V\_SENSE"

Page-9, JDDR1 is change to 10.1mm height  
Page-10, JDDR1 is change to 6.0mm height  
Page-11, L62,L63 are change PART ID by buyer suggestion  
"JLVDS1" reference is change to "UMA\_CN1"  
"CONVERTER\_DPC\_TXP0/1" net name are change to "CONVERTER\_DPD\_TXP0/1"  
"CONVERTER\_DPC\_TXN0/1" net name are change to "CONVERTER\_DPD\_TXN0/1"  
"CONVERTER\_DPC\_AUXP/N" net name are change to "CONVERTER\_DPC\_AUXP/N"

Page-12, C810~C817 are not stuff,R798,R799 are not stuff  
Net "CPU\_GFX\_TXP0~15","CPU\_GFX\_TXN0~15","CPU\_GFX\_RXP0~15" and "CPU\_GFX\_RXN0~15"  
seriacl CAP are change to 0.22uF  
Stuff R802,un-stuff R805 for Nvidia suggestion

Page-13,R838 is stuff,R1143 un-stuff for EC & BIOS suggestion  
Add R1144,C991 for power soft star  
Add net "EC\_SCLK0","EC\_SDAT0" for EDID flash issue

Page-14,Net "PCIE\_TV\_RXN/P" and "PCIE\_TV\_TXN/P" are change connect to PCH PCIE port5  
Net "PCIE\_WLAN\_RXN/P" and "PCIE\_WLAN\_TXN/P" are change connect to PCH PCIE port6  
Net "USB\_OC6#" rename to EC\_SCI# for BIOS suggestion

Page-15,R935 is change to 1K ohm,R331 is change to 0 ohm,R936 is change to 4.7k ohm follow Intel CRB  
R951 and R952 are stuff 10k ohm to disable DDPB,DDPC  
Net "PCH\_DVI\_DATA0~2P/N" are change to DDPC,Net "CONVERTER\_DPDTX0~1P/N" are change to DDPD  
ODD change to connect Net "SATA\_RX4N/P" and "SATA\_TX4N/P"  
R940 and R941 are stuff 10k ohm,R946 and R947 are stuff 10k ohm

Page-16,X5 is changed PART ID by buyer suggestion  
R1123 and R1020 are un-stuff,add R1121 for PCH clear CMOS  
Add JME1 for BIOS request,add R1122 follow Intel CRB

Page-17,L59 is changed PART ID by buyer suggestion  
Page-18,R1069 and R1070 are un-stuff for BIOS & EC suggestion  
Page-19,R934 is un-stuff for can't boot issue  
Page-20,JMIC1 is change PART ID by buyer suggestion  
Page-21,JHP1 and JLINEOUT1 change PART ID by buyer suggestion  
Page-22,Remove Q50 for can't boot issue  
Add 0ohm R1127,R373 is change to 2.2k ohm,Q32 is unstuff  
Page-22,Remove Q50 for can't boot issue  
Add 0ohm R1127,R373 is change to 2.2k ohm,Q32 is unstuff for 100mW issue

Page-23,JCR1 is change PART ID  
JSATAHDD1 is change white color,JSATAODD1 is change blue color

Page-24,R384,R386,R392,R385,R389,R395,R579,R580 and R571 are change to 0805 footprint  
Add 0ohm R621 reset signal for 80 port

Page-25,C921 and C922 are change 18pF for SI pass

Page-26,JUSB30L1,JUSB30L2,JUSBR0~3 and JUSBON1 are change PART ID for ME height request

Page-27,Add R1141,R1142 for S3 wake  
Add manual parts PCB1,CPU\_BACK1,CPU\_STAIN1,CPU HOLDER1,JECSPi2,JFCHSPi2,JUMP1~3 and JRTCBATT2

Page-28,U36 is change G781-1P8f,remove U28,Q41 for address conflick issue  
R471 is un-stuff; R506,R507 are change connect to +3V\_S5  
R466,R467 are change to 10k ohm for <100mW issue

Page-29,Remove R332,R333,R334,R338,R342,R575,R576 and R577  
Page-30,PR5,PR6 are change PART ID for power suggestion  
PR19 is stuff,PR21 is un-stuff for AUDIO headphone in S3 noisy issue  
Reserve PC213 for power suggestion

Page-31,PR41 is change PART ID for power suggestion  
PC46, PR49, PU3, PR48 and PC47 are un-stuff for < 100mW issue

Page-32,PR60 and PR71 are change connect to +3V\_S0  
PR66 and PR77 are change PART ID for power suggestion  
PQ56 is change use BJT for vlotage select issue

Page-33,PR82 is change connect to +3V\_S0 ; PR88 PART ID is change,Add PR274 for CPU voltage sense  
PQ58 is change use BJT for vlotage select issue

Page-35,PR134 is un-stuff for power sequence issue  
Page-36,PR260 is change PART ID for power suggestion

PVT & MP de-pop circuit

page 16 for EC debug connector  
JECDB1

page 17 for HP debug  
JLPCDB1,R310,JHPDB5,C147,U31,Q22,D9~D14,R312~R317

page 17 for AMD debug  
U5,R53,R56,R77,R80

page 17 for TnI HW debug (CRT output function)  
C3,C4,C7,C14,C15,C16,C21,C22,D22,D23,JCRTDB1  
L1,L2,L3,Q1,Q2,R1,R2,R3,R4,R5,R6,R10,R11,R14  
R15,R25,R26,R28,R29,R30,R32,R36,R37,U1,U2

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXX		remark	<remark>
Date	Tuesday, May 06, 2012	Sheet	43	of	43	